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Self-Assembled Nanodielectrics and Combustion Processed Amorphous Metal Oxides as Unconventional Materials for Thin-Film Transistors

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Abstract

Self-Assembled Nanodielectrics and Combustion Processed Amorphous Metal Oxides as Unconventional Materials for Thin-Film Transistors

Katie Lynn Stallings

The demand for low cost, unconventional electronics requires new materials with unique characteristics that the traditionally used silicon-based technologies cannot provide. Metal oxide semiconductors, such has amorphous indium gallium zinc oxide (a-IGZO), have made impressive strides as alternatives to amorphous silicon for electronics applications. However, to achieve the full potential of these semiconductors, compatible unconventional gate dielectric materials must also be developed. To this end, solution-processable self-assembled nanodielectrics (SANDs) comprised of structurally well-defined and durable nanoscopic alternating organic (e.g., stilbazolium) and inorganic oxide (e.g., ZrO_x, HfO_x) layers offer impressive capacitances and low processing temperatures ($T \leq 200$ °C). Amorphous metal oxides have already been utilized in manufactured displays, but conventional processing techniques require expensive high vacuum deposition or high annealing temperatures that are incompatible with low-cost plastic substrates. The combustion process was developed to provide a low temperature solution-based fabrication process. This research has focused on further developing these promising unconventional materials and processing method.

In Chapter 2, the role of the organic layer component in the SAND structure is explored. SANDs are compatible with a wide variety of semiconductors and often enable superior thin-film transistor (TFT) device metrics in comparison to analogous inorganic dielectrics. This has been partly attributed to the interactions of the organic layers. To help determine the role of the stilbazolium derived organic layer (**Chr**) previously used, a new hydrocarbon chain based self-assembly molecule (**Alk**) was developed. By using **Alk** and **Chr** in differing organic layers, the effects of the highly polarizable **Chr** molecule's built-in dipole on the overall SAND characteristics is better understood. The different layer identity and arrangement of the organic layers within the Zr-SAND structure is found to have a significant impact on the leakage behavior of the capacitors and the threshold voltage/turn-on voltage of pentacene transistors. Evidence of interactions between adjacent **Chr** organic layers enhancing these effects is also observed.

Chapter 3 demonstrates the capabilities of SANDs to be applied to more complex device architectures. While SANDs have been paired with diverse semiconductors and yielded excellent device metrics, they have never been implemented in the most technologically relevant top-gated thin-film transistor (TFT) architecture. Here we combine solution-processed a-IGZO with solution-processed four-layer Hf-SAND dielectrics to fabricate top-gated TFTs, which exhibit impressive electron mobilities (μ_{SAT} = 19.4 $cm^2\ V^{-1}\ s^{-1}$) as well as low threshold voltages (V_{th} = 0.83 V), subthreshold slopes (SS = 293 mV/dec), and gate leakage currents (10^{-10} A).

Chapter 4 examines the performance and thermal stability of indium gallium oxide fabricated by pulsed laser deposition (PLD), and the solution-based combustion synthesis for both spin-coated and spray-coated films over a range of compositions. To leverage the existing knowledge base on amorphous oxides, this study directly compares one of the most promising

solution processing techniques, combustion synthesis, with a more established PVD growth technique, pulsed laser deposition (PLD). The roles of processing technique and composition are understood by coupling structural studies, including analysis of local bonding and density, with existing literature of PVD amorphous oxide films. This work represents the first example of X-ray absorption spectroscopy analysis of spray combustion processed (Spray-CS) a-oxide films. A drop in TFT saturation mobility, with increasing Ga content, for PLD and spin-coated combustion processed (Spin-CS) devices is understood to be the disruption of carrier mobility imposed by the disparate local structure around Ga, as opposed to around indium. In contrast, saturation mobility for Spray-CS films is dominated by the processing method and cannot be tuned with composition. Similar to mobility trends, TFT on voltage rises with Ga content for Spin-CS and PLD-derived channel layers. Local structure studies reveal that the Spray-CS growth technique results in high In-O coordination levels, which explains the low carrier concentrations and resultant on voltage behavior. This work investigates, for the first time, the structural phase stability of solution-processed oxides through *in situ* glancing incidence X-ray diffraction annealing studies. Thermal phase stability, which informs processing parameters and device stability, is shown to increase with Ga content for all films.

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List of Abbreviations

AAC	Three-layer Zr-SAND Structure with Two Alk Organic Layer Followed by One Chr Organic Layer
ACA	Three-layer Zr-SAND Structure with an Alk Organic Layer, a Chr Organic Layer, and an Alk Organic Layer
ACC	Three-layer Zr-SAND Structure with an Alk Organic Layer Followed by Two Chr Organic Layers
AFM	Atomic Force Microscopy
a-IGO	Amorphous Indium Gallium Oxide
a-IGZO	Amorphous Indium Gallium Zinc Oxide
ALD	Atomic Layer Deposition
Alk (A)	11-Hydroxyundecylphosphonic Acid
a-MO	Amorphous Metal Oxide
a-TCO	Amorphous Transparent Conducting Oxide
At. %	Atomic Percent
CAA	Three-layer Zr-SAND Structure with a Chr Organic Layer Followed by Two Alk Organic Layers
CAC	Three-layer Zr-SAND Structure with a Chr Organic Layer, an Alk Organic Layer, and a Chr Organic Layer
CCA	Three-layer Zr-SAND Structure with Two Chr Organic Layers Followed by an Alk Organic Layer

Chr (C)	Chromophore (4-[[4-[Bis(2-Hydroxyethyl)Amino]Phenyl]Diazenyl]-1-[4-(Diethoxyphosphoryl) Benzyl] Pyridinium Bromide)
C_i	Capacitance per Unit Area of the Gate Dielectric
C-f	Capacitance-Frequency
CS	Combustion Synthesis
CS-TEM	Cross-Sectional Transmission Electron Microscopy
C-V	Capacitance-Voltage
d	Dielectric Thickness
D_{bulk}	Bulk Trap Density
DC	Direct Current
ΔV_{th}	Threshold Voltage Shift
D_{it}	Interfacial Trap Density
e	Elementary Charge
EDS	Energy-Dispersive Spectroscopy
EF	Electric Field
ε_0	Permittivity of Vacuum
EXAFS	Extended X-ray Absorption Fine Structure
FIB	Focused Ion Beam
GIXRD	Glancing Incidence X-ray Diffraction
G-V	Conductance-Voltage
HEPA	High Efficiency Particulate Air
Hf-SAND	Hafnia Self-Assembled Nanodielectric

I	Current
I_c	Area Under Crystalline Diffraction Peaks
I_{DS}	Source-Drain Current
I_{on}:I_{off}	On Current to Off Current Ratio
ITO	Indium Tin Oxide
I_{total}	Area Under the Background-Subtracted, Total Scattering Pattern
I-V	Current-Voltage
J	Leakage Current Density
J-V	Leakage Current Density-Voltage
k	Dielectric Constant
k_B	Boltzmann Constant
k_{eff}	Effective Dielectric Constant
L	Channel Length
MIM	Metal-Insulator-Metal
MIS	Metal-Insulator-Semiconductor
μ_{SAT}	Saturation Mobility
OTFT	Organic Thin-Film Transistor
OTS	Octadecyltrichlorosilane
PAE	4-[[4-[Bis(2-Hydroxyethyl)Amino]Phenyl]Diazenyl]-1-[4-(Diethoxyphosphoryl) Benzyl] Pyridinium Bromide
P_{cryst}	Crystalline Fraction
PECVD	Plasma-Enhanced Chemical Vapor Deposition

PLD	Pulsed Laser Deposition
ρ	Electron Density
ρ_{Si}	Electron Density of Silicon
PVD	Physical Vapor Deposition
P(VDF)-TrFE)	Poly(Vinylidene Fluoride-Trifluoroethylene)
RF	Radio Frequency
rms	Root Mean Square
SAND	Self-Assembled Nanodielectric
Spin-CS	Spin Combustion Synthesis
SOG	Spin-on-Glass
Spray-CS	Spray Combustion Synthesis
SS	Subthreshold Slope
T	Temperature
TFT	Thin-Film Transistor
TG-BC	Top-Gate Bottom-Contact
TG-TC	Top-Gate Top-Contact
T_{MAX}	Maximum Temperature
T_{onset}	Onset of Crystallization
UV-Vis	Ultraviolet-Visible Spectroscopy
V_{DS}	Source-Drain Voltage
V_G	Gate Voltage
V_{on}	Turn-On Voltage

V_{th}	Threshold Voltage
W	Channel Width
XAS	X-ray Absorption Spectroscopy
XPS	X-ray Photoelectron Spectroscopy
XRF	X-ray Fluorescence Spectroscopy
XRR	X-ray Reflectivity
Zr-SAND	Zirconia Self-Assembled Nanodielectrics

Table of Contents

List of Figures

List of Tables

Chapter 1

Introduction to Thin-Film Transistors, Combustion Processing, and Self-Assembled Nanodielectrics

1.1 Thin-Film Transistors (TFTs)

Transistors, whether in simple or complex integrated circuits, are ubiquitous in and considered to be the most important component of modern electronics.[1] Transistors act as basic switches where current flow is controlled by the application of an electric field produced by a voltage. The importance of the transistor is highlighted by Moore's Law, which states that the number of transistors per microchip will double every eighteen months.[2] For many decades, transistor technology was dominated by Si/SiO_2 materials such as amorphous silicon (a-Si) and low-temperature polycrystalline silicon (LTPS). However as the demand for lower power usage, higher resolution, and larger screen size increased, silicon based materials reached the limits of their scalability.[1, 3-4] The search for new, unconventional materials to replace silicon led to metal oxides (MOs) among others.[2, 4] The unique structure of metal oxides has opened up further possibilities and applications for which silicon is not suited, such as transparent and/or flexible electronics produced by low-cost solution-processing.

1.1.1 TFT Operation

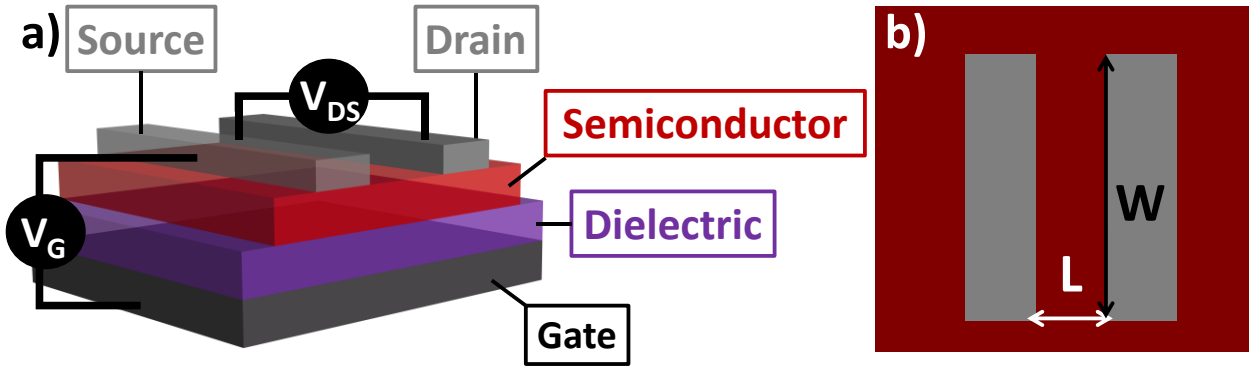

Figure 1.1. Basic Thin-Film Transistor Design. a) A typical bottom-gate top-contact TFT. A gate voltage (V_G) is applied between the source and gate electrodes, and a source drain voltage (V_{DS}) is applied between the source and the drain electrodes. b) View of a bottom-gate top-contact TFT from above showing the device's length (L) and width (W).

Thin-film transistors are field-effect devices that are made of three main components: electrodes, semiconductors, and dielectrics (Figure 1.1 a).[1-2] TFTs are also three terminal devices, meaning that there are three electrodes the source, the drain, and the gate, which are made of conductive materials.[1-2] The source and drain electrodes are in direct contact with the semiconductor while the gate is separated from it by the dielectric.[1] The length (L) of a transistor is the space between the source and the drain, and the width (W) is the distance that the source and drain run parallel (Figure 1.1 b).[1] Both of these parameters are important to device function and the calculation of device metrics. When a voltage is applied between the source and gate electrodes (V_G), the dielectric becomes polarized and induces charges that begin accumulating at the dielectric/semiconductor interface, which is known as the field-effect.[1-2] The voltage induced charge is only present in the first 1-2 nm of the semiconductor at the dielectric/semiconductor

interface and is known as the accumulation layer.[5] When a V_G and a voltage between the source and the drain (V_{DS}) are both applied, the charges begin to flow in the accumulation layer between the source and drain forming the channel, and the resulting current is termed I_{DS} (Figure 1.1 a).[1] Ideally when a V_{DS} is applied, no current flows if a V_G is not also employed. TFTs are classified by the type of charge that is generated in the semiconductor and subsequently forms the channel. In p-type transistors, positively charged holes produce the I_{DS} when negative voltages are applied. For n-type transistors, negatively charged electrons form the channel and current flows when positive voltages are applied. Ambipolar transistors have significant amounts of both holes and electrons, which charges produce the I_{DS} is thus dependent on whether positive or negative voltages are applied.

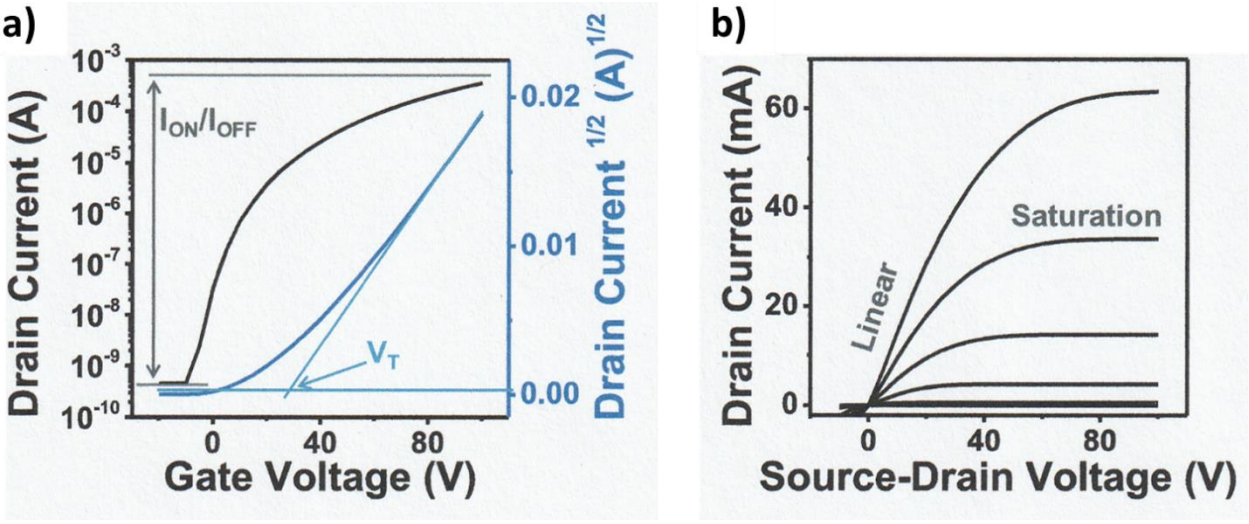

Figure 1.2. Basic TFT Electrical Measurements. a) Representative TFT transfer plot. The derivation of the threshold voltage (V_{th}) and on/off current ratio are shown. b) Representative output plot for a TFT. The linear and saturation regimes are identified. Adapted from Hennek.[6]

There are two main electrical measurements used to characterize TFTs: transfer and output (Figure 1.2). Transfer measurements record I_{DS} as a function of V_G at constant V_{DS} (Figure 1.2 a). Output measurements trace I_{DS} as a function of a fixed V_G while sweeping V_{DS} (Figure 1.2 b). From transfer curves, TFT device metrics such as mobility (μ), threshold voltage (V_{th}), turn-on voltage (V_{on}), the ratio of the on current to the off current (I_{on}:I_{off} or on/off), and the subthreshold slope (SS) can be extracted. The current flowing between the source and drain can be measured in either the linear or saturation mode. When V_{DS} is significantly lower than V_G, there is a linear relationship between the current and the voltage, thus it is termed the linear regime.[1] When V_{DS} is comparable to V_G, the field across the dielectric is not strong enough to maintain the accumulated charges in the area of the drain, which becomes depleted. The channel is then considered to be "pinched off." When this occurs, the current becomes independent of V_{DS}, and the device is operating in saturation mode.[1] These two modes are described in the following equations:

$$I_{DS_{LIN}} = \left(\frac{W}{L}\right)\mu C_i\left(V_G - V_{th} - \frac{V_{DS}}{2}\right)V_{DS}$$

$$I_{DS_{SAT}} = \left(\frac{W}{2L}\right)\mu C_i(V_G - V_{th})^2$$

where *W* is the channel width, *L* is the channel length, and C_i is the capacitance per unit area of the dielectric.[1]

The mobility (μ) is related to how efficiently a charge carrier can be transported through a material.[2] Mobility can be significantly affected by scattering from structural defects in the semiconductor such as impurities and grain boundaries. Because the charge transport in TFTs takes place at the dielectric/semiconductor interface, this interface is of the utmost importance.

Dielectric effects on mobility include scattering from dielectric charges, interfacial states, and surface roughness.[2]

The threshold voltage (V_{th}) is the gate voltage at which the channel is formed allowing for charges to flow between the source and the drain.[2] In equations for I_{DS}, the V_{th} helps account for any offset in the accumulation or depletion of charges that impact the transport in the channel.[1] The excess or dearth of charges in the semiconductor can be caused by donor or acceptor states and bulk charges in the semiconductor, even at zero gate voltage, as well as trapping at the dielectric/semiconductor interface.[1] For a n-type TFT, if V_{th} is negative, the device is in depletion mode, and if it is positive, the device is in enhancement mode. Preferably a TFT will operate in enhancement mode as the application of a gate voltage is not required to turn the device off.[2] The turn-on voltage (V_{on}) is the gate voltage required to turn a device to the on state.[1-2] V_{th} and V_{on} are very similar in definition but are calculated in significantly different ways. V_{on} is the gate voltage at which I_{DS} begins to increase as shown by a log(I_{DS}) vs. V_G plot (Figure 1.2 a).[2] V_{th} can be derived from the saturation mobility equation by plotting $I_{DS}^{1/2}$ vs. V_G. The intercept on the voltage axis of the linear portion of the plot can be extrapolated, which gives V_{th} (Figure 1.2 a).[1] It is desirable for both V_{th} and V_{on} to be as close to zero volts as possible so that a minimal amount of voltage is required to turn a device to the on state. This translates to lower power consumption for device operation.

The I_{on}:I_{off} is the ratio of the maximum drain current (on current) to the minimum drain current (off current).[2] The maximum I_{DS} is dictated by the effectiveness of the dielectric to induce charges and on the movement of the charges through the semiconductor material. The minimum I_{DS} is ideally given by the gate leakage current (I_G) through the dielectric. The I_{on}:I_{off} should be as

large as possible, at least 10^6, because the difference between the on and off states determines the successful usage of the TFT as an electronic switch.[2]

The subthreshold slope (SS) is a measure of how much voltage is required to turn a device from the off to the on state.[7] Specifically, the SS is the amount of voltage needed to increase the I_{DS} by one decade.[2] The SS relates to the dielectric/semiconductor interface's electronic quality and is a measure of how efficiently the channel is formed.[1] The SS should be as small as possible because this results in reduced operating voltage and thus lowers the power consumption and increases switching speeds.[2, 7]

1.1.2 Device Architecture

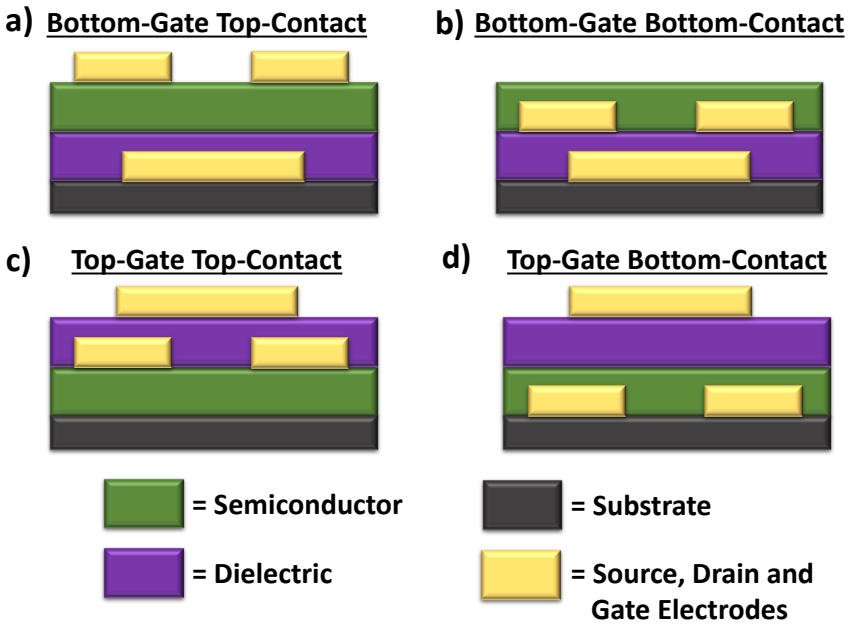

Figure 1.3. Four Basic TFT Device Architectures. Bottom-gate top-contact (BG-TC) (a), bottom-gate bottom-contact (BG-BC) (b), top-gate top-contact (TG-TC) (c), and top-gate bottom-contact (TG-BC) (d) device structures.

There are many different device architectures for TFTs,[7] but only the four main types, as shown in Figure 1.3, will be discussed here. The architectures are named following two conventions: 1) the position of the gate and contacts in relation to the semiconductor and 2) the position of the source and drain in relation to the gate. When the gate is above the semiconductor, the device is classified as top-gate (TG), and when the gate is below the semiconductor, the device is termed bottom-gate (BG). Similarly, when the contacts are positioned above the semiconductor, it is referred to as top-contact (TC), and when the contacts are below the semiconductor, the device is called bottom-contact (BC). When the contacts are on the same side of the semiconductor as the gate, the device is coplanar as in TG-TC and BG-BC devices (Figure 1.3 b and c). The devices are staggered when the contacts and gate are on opposite sides of the semiconductor as in BG-TC and TG-BC (Figure 1.3 a and d).

Each configuration has its own advantages and disadvantages. The most commonly used structure in research is BG-TC due to the ease of fabrication. It was also the first architecture to be studied.[7] It allows for the deposition of the semiconductor onto a flat and stable surface and requires minimal if any lithography. However BG-TC devices are not typically used in industrial applications as the significant overlap between the contacts and the gate results in high parasitic capacitance which greatly reduces the switching speeds of devices.[7] In BG architectures, the semiconductor back-channel is exposed to the environment, which can require an additional encapsulation layer, complicating fabrication. In BG-TC devices, specifically, the semiconductor can be damaged in the deposition of contacts.[7] In top-gate TFTs the dielectric itself can also serve as an encapsulation layer to prevent environmental contaminants as well as a light shield if the material is opaque.[7] Coplanar devices have lower contact resistance due to the minimal contact

between the source and drain and the semiconductor. Also, epitaxial growth of crystalline devices is much easier for coplanar architectures.

Additional considerations in device fabrication include lithography and patterning. If the W/L ratio of the contacts is small (<10), then fringe effects can prevent the accurate assessment of the mobility.[3] The fringe effect occurs when currents follow between the contacts outside of the defined contact region; this results in the W not being defined by the contact dimensions and actually being underestimated which causes the mobility to be overestimated.[3] The fringe effect can also be prevented by the careful patterning of the semiconductor via lithography allowing for smaller W/L ratios. Lithography can also be used to reduce or eliminate parasitic capacitance by minimizing the overlap between the contacts and gate.

1.2 Metal Oxide Semiconductors

1.2.1. Comparison of Silicon and Metal Oxides

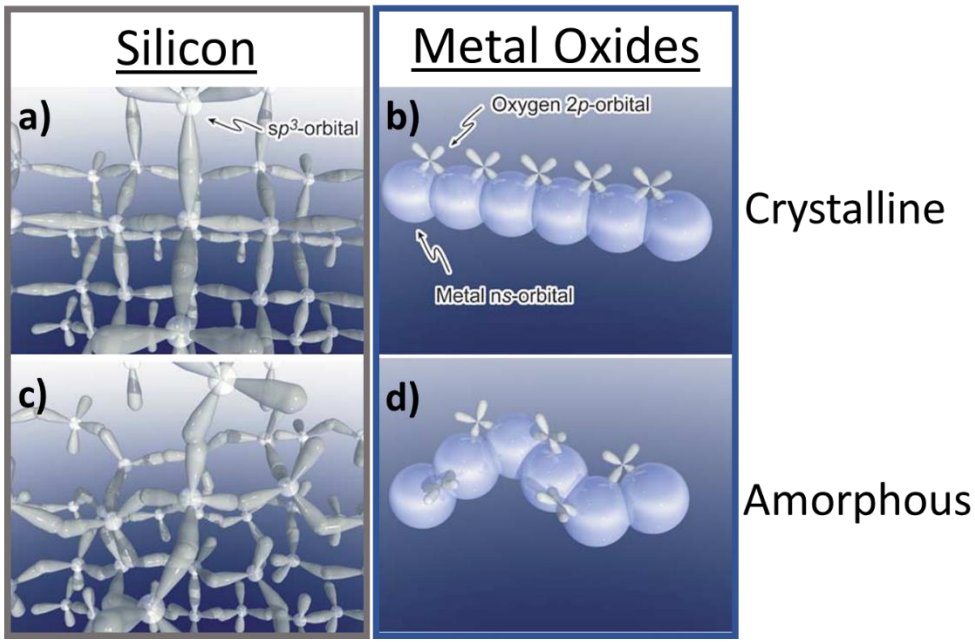

Figure 1.4. Orbital Structures of Silicon and Metal Oxides. In crystalline silicon, the regular overlap of the sp^3 hybridized orbitals forms the conduction band (a). For crystalline metal oxides, the spherical ns orbitals make-up the conduction band (b). When silicon is in the amorphous state the overlap of the sp^3 orbitals is disrupted leading to significant drops in mobility (c). Due to the spherical nature of the metal ns orbitals, the orbital overlap and thus the conduction pathway is maintained in the amorphous state (d). Adapted from Nomura.[8]

In silicon, the conduction band is composed of anisotropic, covalent sp^3 hybridized orbitals.[1, 9] The band gap is the separation between the conduction band minimum and valence band maximum formed by the antibonding and bonding hybridized orbitals respectively.[1] When silicon is in the crystalline state, the overlapping sp^3 orbitals form a well-ordered conduction

pathway which produces high mobilities in TFTs (Figure 1.4 a).[7] However when the crystalline structure is disrupted as it is in a-Si or by nonoptimized processing, the conduction pathway is broken and large amounts of tail and localized states form in the band gap due to dangling bonds forcing the electrons to hop between orbitals (Figure 1.4 c).[1, 7, 9] The changes in the silicon structure between the crystalline and amorphous states lead to approximately a thousand fold drop in the mobility to ~1 $cm^2\ V^{-1}\ s^{-1}$.[9]

For metal oxides the conduction band is formed by the overlap of the large s orbitals of transition metal cations with the structure $(n-1)d^{10}ns^0$ ($n \geq 4$) such as indium, zinc, and tin (Figure 1.4 b).[7] Due to the spherical nature of the s orbitals, the structure is significantly less sensitive to lattice distortion even when going from the crystalline to amorphous state (Figure 1.4 d).[7] The amorphous structure of MOs results in large area uniformity, ultrasmooth surfaces, and no grain boundaries, which helps prevent interface traps and scattering centers as seen in polycrystalline films such as LTPS.[2-3, 10] Flexible electronics are also possible with amorphous MOs (a-MOs) due to the high mobilities (~10-50 $cm^2\ V^{-1}\ s^{-1}$) achievable at low processing temperatures allowing for the use of inexpensive plastic substrates.[2-3, 10] A further advantage of MOs is the wide bandgaps (~3.5 eV) resulting in transparency, which is not possible in opaque Si.[3, 9-11]

1.2.2 Traditional Metal Oxide Processing

As with silicon semiconductors, vapor deposition techniques, such as pulsed laser deposition (PLD) and rf-magnetron sputtering, have been widely used to fabricate MO films.[9] Vapor deposited MOs have produced TFTs with V_{th} near 0 V, large I_{on}:I_{off} (>10^7), and mobilities larger than 50 $cm^2\ V^{-1}\ s^{-1}$.[9] Vapor deposition, particularly in the early development of MOs, had

the advantages of tool availability, industrial fabrication infrastructure compatibility, and low-temperature deposition.[7] However vapor deposition is high cost, needs lithography for complex device fabrication, is restricted to relatively small areas, meaning it is incompatible with large area electronics, and, depending on the technique, is difficult to tune compositionally.[3]

Because the conduction band structure of MOs is significantly less sensitive to lattice distortion, excellent TFT metrics can be achieved via solution-processing. Solution-processing has long been of interest because it allows direct additive patterning, in which materials are only deposited where they are wanted, eliminating the need for lithography and significantly reducing materials waste.[2, 10] Therefore, solution-processing can ultimately result in low-cost, high throughput fabrication on flexible plastic substrates.[9] The composition of precursor solutions can also be easily tuned allowing for greater adaptability.[9] Further benefits of solution-processing are fabrication under atmospheric conditions allowing for simpler equipment, and scalability for large area applications.[3, 12]

The traditional solution-processing route is sol-gel deposition.[3] In this method the liquid precursors become a colloidal suspension known as a sol and then a network structure referred to as a gel.[3] When the metal salts are dissolved, the metal cations form metal hydroxides with deprotonated solvent.[3] The metal hydroxides are then condensed to form a metal-oxygen-metal (M-O-M) network via heating.[3] The annealing step of solution-processing achieves condensation, impurity removal, and film densification.[3] In condensation the metal-oxygen-metal (M-O-M) structure is formed. During impurity removal, the solvents and byproducts are removed by decomposition and evaporation. In film densification, voids are removed.[3] Annealing temperatures of greater than 400 °C are typically required to achieve acceptable film performance, which

prevents the implementation of plastic substrates.[3, 10, 13] This limitation of traditional sol-gel chemistry has led to a need for unconventional solution-processing methods to utilize all of the unique properties of metal oxides.[3]

1.2.3 Combustion Processing of Metal Oxides

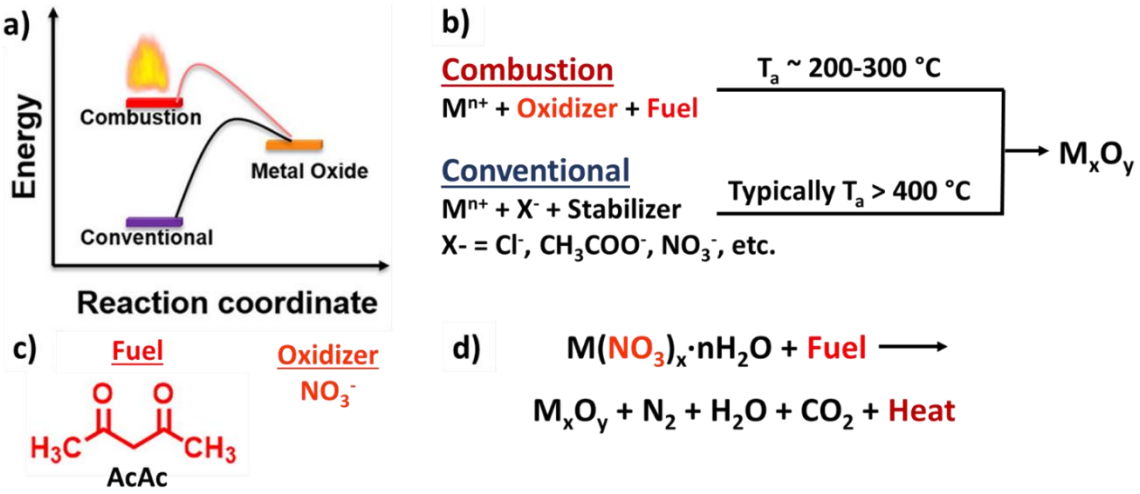

Figure 1.5. Combustion Synthesis Basics. a) Comparison of the energetics for combustion and traditional processing of metal oxides. b) Depiction of precursor components and annealing temperature for combustion and traditional processes. c) The fuel (acetylacetone, AcAc) and oxidizer components of combustion processing. d) Idealized combustion synthesis reaction. Note that not all the species in the reaction have been identified. Figure partially adapted from Chen[14] and Wang.[15]

To reduce the processing temperature required for MO lattice formation, the Marks' group developed combustion synthesis (Figure 1.5).[13] In the combustion process a fuel and an oxidizer are included in the precursor solutions.[13] The resulting self-catalytic redox reaction is highly exothermic and helps to form the M-O-M network and remove organic impurities at significantly

lower annealing temperatures.[13, 16] The oxidizer is provided by the nitrates from the metal salts used to prepare the precursor solutions. The fuel, typically acetylacetone (AcAc), is added along with ammonia, which assists in fuel coordination with the metal cations.[13, 16] The presence of the oxidizer helps to remove organic impurities without the formation of coke, which is sometimes seen in bulk combustion reactions.[13]

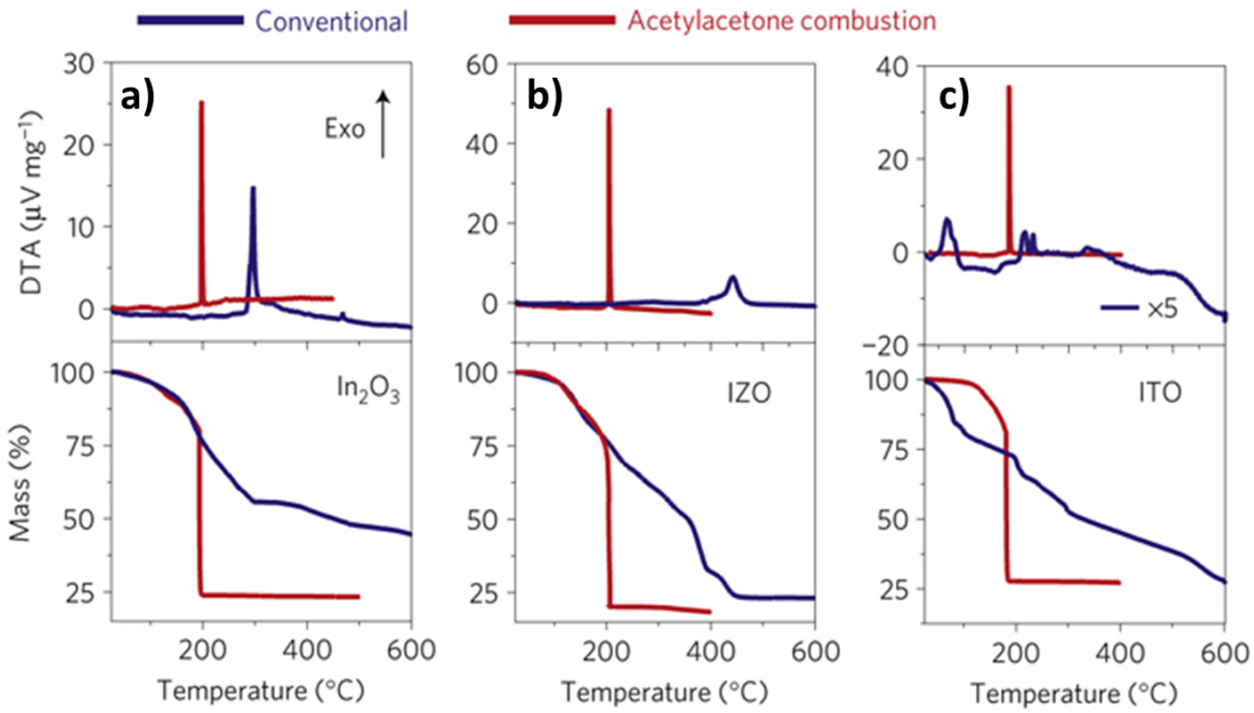

Figure 1.6. TGA and DTA Analysis of Combustion and Traditional Precursors. Conventional precursors are shown in blue and combustion precursors are shown in red for a) indium oxide, b) IZO, and c) ITO. The exotherms for the combustion precursors are sharper and occur at earlier temperatures than the conventional ones. Combustion precursors also show abrupt mass loss while the traditional precursors undergo slower and gradual mass loss. Adapted from Kim.[13]

Thermogravimetric analysis (TGA) and differential thermal analysis (DTA) were used to compare conventional and combustion precursors (Figure 1.6).[13] Broad endotherms relating to

lattice formation followed by exotherms corresponding to organic removal are seen for the conventional precursors.[13] In contrast, the combustion precursors have a single sharp exotherm with a corresponding large mass loss.[13] These analyses reveal that the combustion precursors require significantly lower conversion temperatures (<200 – 300 °C) than the conventional systems (>500 – 600 °C).[13] The combustion process was successfully applied to a number of metal oxides, such as indium oxide, zinc tin oxide (ZTO), indium zinc oxide (IZO), and indium tin oxide (ITO), demonstrating its wide compatibility. Time-of-flight secondary ion mass spectrometry (ToF-SIMS) of combustion processed In_2O_3 showed an In^+/CH_3^+ intensity ratio of approximately 10,000 inside of the film, which is the noise level of the measurement.[13] This means that there is exceptionally low carbon contamination within the film as a result of efficient organic removal by the combustion process.[13] The smooth and contiguous films produced by the combustion process were confirmed by atomic force microscopy (AFM) and scanning electron microscopy (SEM).[13] X-ray photoelectron spectroscopy (XPS) was also used to evaluate the combustion and conventionally processed films. XPS is essential to determining the quality of metal oxide lattice formation.[16] The O 1s peak can be deconvoluted into three separate peaks: M-O-M lattice (529.9 eV), metal-OH (531.2 eV) and adsorbed surface species (532.3 eV).[16-17] The fraction of the M-O-M lattice peak to the overall O 1s peak ($\eta_{M\text{-}O\text{-}M}$) is used to assess the extent of the formation of the desired M-O-M network and can be compared between films. XPS measurements confirm higher $\eta_{M\text{-}O\text{-}M}$ for combustion processed films than traditional sol-gel ones (Figure 1.7).[13] Significantly this study demonstrated an In_2O_3/a-alumina TFT on an AryLite polyester substrate annealed at 200 °C with an impressive μ_{SAT} of 6 $cm^2\ V^{-1}\ s^{-1}$ thus showing that combustion processing lowers the annealing temperature for high quality MOs to be compatible with flexible substrates.[13]

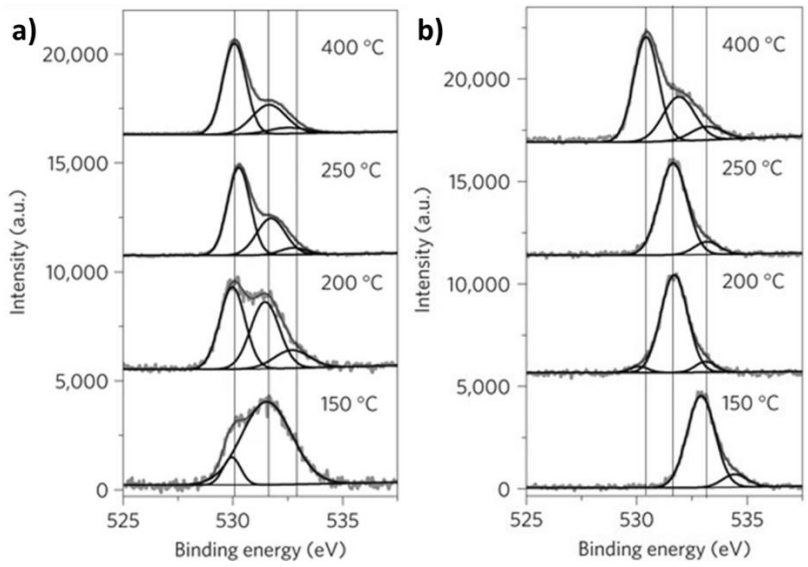

Figure 1.7 XPS O 1s Analysis of Combustion and Conventional Processed Films. The O 1s peak is deconvoluted into M-O-M, M-OH, and absorbed oxygen species for a) combustion and b) conventionally processed indium oxide films at various annealing temperatures. Adapted from Kim.[13]

Combustion Fuels

In addition to the metal nitrate salts, AcAc, and 2-methoxyethanol solvent, combustion precursor solutions also contain ammonia to promote the deprotonation of the AcAc, which allows it to coordinate with the metal cations (M^+) through the negatively charged oxygens. In optimization studies, the best performance was achieved with a metal cation, AcAc, and ammonia ratio of 1:2:1.

A further study on combustion processing focused on the pre-decomposition of the precursors in AcAc and nitrate systems to better understand the nature of the reaction.[16] TGA/DTA studies of various AcAc-nitrate systems demonstrated that 150 °C is the minimum temperature

required for the initiation of the combustion reaction.[16] Initiation is achieved in shorter amounts of time at higher temperatures (5 minutes at 175 °C compared to 35 minutes at 150 °C).[16] TGA-MS (mass spectrometry) demonstrated the initial mass loss and decomposition of the organic fuels in a continuously heated sample by identifying the products as CH_3CO, CO_2, CH_3COCH_3, O, and NO.[16] The existence of highly oxidizing species such as O and NO, which are not present in non-combustion processes, increases the decomposition rate of the organics to CO_2.[16] The delay in initiation times at lower temperatures is attributed to the slower build-up of oxidizing species needed to begin combustion synthesis.[16] The complete oxidation of the organics produces significant amounts of H_2O, CO_2, NH_3, NO, and O_2 gasses.[16] It should be noted that the combustion process cannot be initiated without sufficient amounts of the fuel and oxidizer present, and the significant loss of oxidizer and fuel as a result of nonoptimal film thickness is a concern.[16]

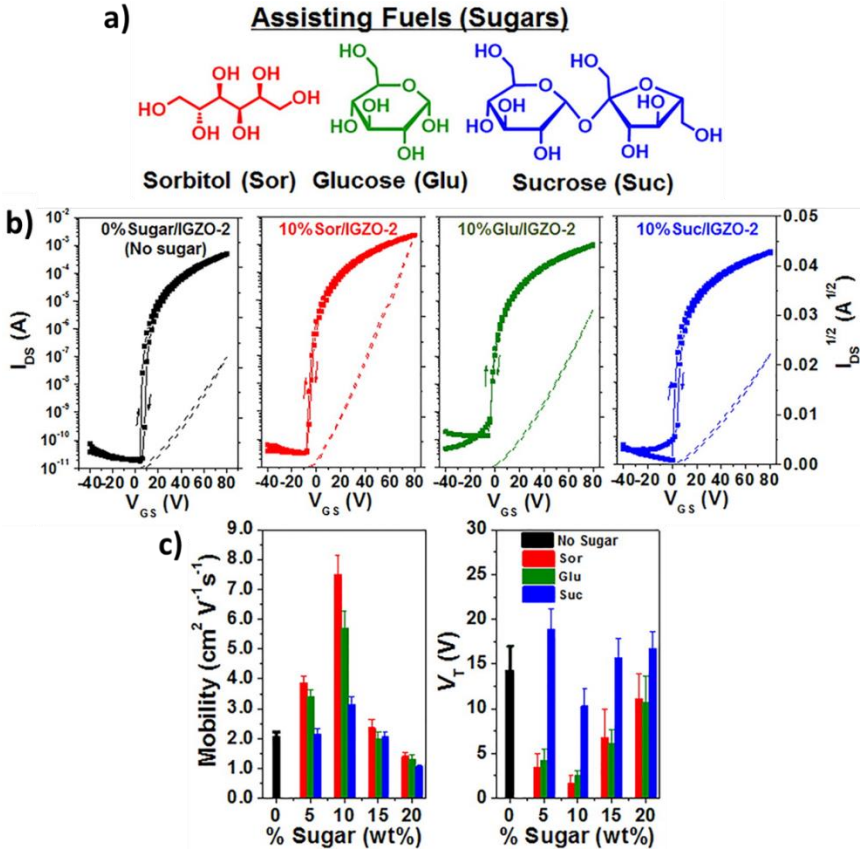

Figure 1.8. Sugars as Cofuels for Combustion Processing. a) Structures of sorbitol, glucose, and sucrose. b) Representative transfer curves for IGZO TFTs fabricated with AcAc only and 10 wt. % of indicted sugar. c) Mobility and V_{th} statistics of IGZO TFTs as a function of sugar wt. % and identity. Adapted from Wang.[15]

Given the impressive results achieved with combustion processing using AcAc as a fuel, other potential fuel molecules have gained interest. Due to wide availability, low cost, and environmental friendliness, the carbohydrates sorbitol, glucose, and sucrose (Figure 1.8 a), were investigated as fuels for combustion processing.[15] Devices produced from precursors containing only the sugars and no AcAc were non-functional.[15] However, precursor solutions with AcAc and any of the sugars produced working devices.[15] This indicates that the AcAc acts as a coordinating

ligand and primary fuel while the sugar is a supporting fuel.[15] The optimum ratio of metal cations to AcAc (M^+:AcAc) is 1:2 without sugars, but with the addition of sugar the best M^+:AcAc becomes 1:4.[15] The TFT performance is also dependent on the identity of the sugar and weight percent (wt. %) of the sugar in solution (Figure 1.8 b and c).[15] The mobility maximizes and V_{th} minimizes with a sugar wt. % of 10.[15] XPS derived $\eta_{M\text{-}O\text{-}M}$ and extended x-ray absorption fine structure (EXAFS) determined indium coordination number (N_i) also both peak at 10 wt. % sugar.[15] These analyses confirm that metal oxide film density is increased with optimal sugar concentration.[15] The thermal analysis of the precursor solutions demonstrates that the addition of the sugars substantially effects the combustion process.[15] All of the sugars lower the ignition temperature (T_{exo}), which is where large mass loss occurs and gaseous products are emitted, and the sugar identity dictates the combustion enthalpy (ΔH_{exo}).[15] High ΔH_{exo} resulted in lower residue weights for the samples, higher mobilities in indium gallium zinc oxide (IGZO) TFTs, and increased metal oxide densification, which is the first time this correlation had been seen.[15] No correlation between the T_{exo} and ΔH_{exo} was observed.[15] Sorbitol produces the cleanest IGZO films with the highest mobility (μ_{SAT} = 8.2 $cm^2\ V^{-1}\ s^{-1}$), and the lowest threshold voltage shift (ΔV_{th}) in bias stress testing.[15]

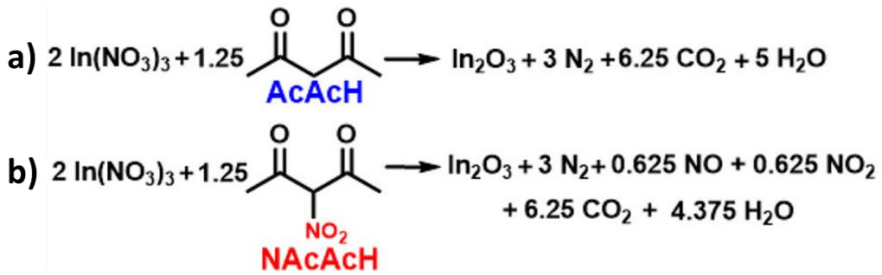

Figure 1.9. Balanced Combustion Process Equations. Balanced combustion process with AcAc (a), and NAcAc (b) as fuels. The structures of AcAc and NAcAc are shown. Adapted from Chen.[14]

Another alternative fuel studied was 3-nitroacetylacetone (NAcAc).[14] NAcAc has a lower ignition temperature (107.8 °C) and a higher enthalpy of combustion (988.6 J/g) than AcAc (166.5 °C and 784.4 J/g).[14] Additionally NAcAc incorporated an oxidizing NO_2 group into the coordinating AcAc structure so that potentially a single oxidizer-fuel-metal complex would be formed in solution. However pure NAcAc metal complexes were not possible due to the poor coordination of the NAcAc. The lack of NAcAc ligation is attributed to the reduced electron density on the coordinating oxygens due to the electron withdrawing ($-NO_2$) group and the tridentate nature of the complexes. Precursor solutions prepared with metal acetates and NAcAc did not undergo a combustion reaction showing that NAcAc does not act as a fuel-oxidizer pair, thus metal nitrate salts were utilized in the further study of NAcAc as a fuel. TGA and DTA experiments confirmed that precursor solutions made with NAcAc resulted in lower combustion initiation temperatures than those prepared with AcAc.[14] IGZO TFTs made with NAcAc as the fuel had better performance and higher $\eta_{M\text{-}O\text{-}M}$ than those produced with AcAc alone. However, the best performance was achieved by mixing the NAcAc and AcAc fuels. The optimal ratio of metal cations to AcAc and NAcAc (M^+:AcAc:NAcAc) was found to be 1:1.5:0.5. This combination produced the highest mobility, better bias stress stability, the highest $\eta_{M\text{-}O\text{-}M}$, and the highest film density in IGZO TFTs.[14] The studies on fuel combinations of NAcAc and AcAc indicate that optimized combustion reactions are a balance between heat generation and gas emission (Figure 1.9).

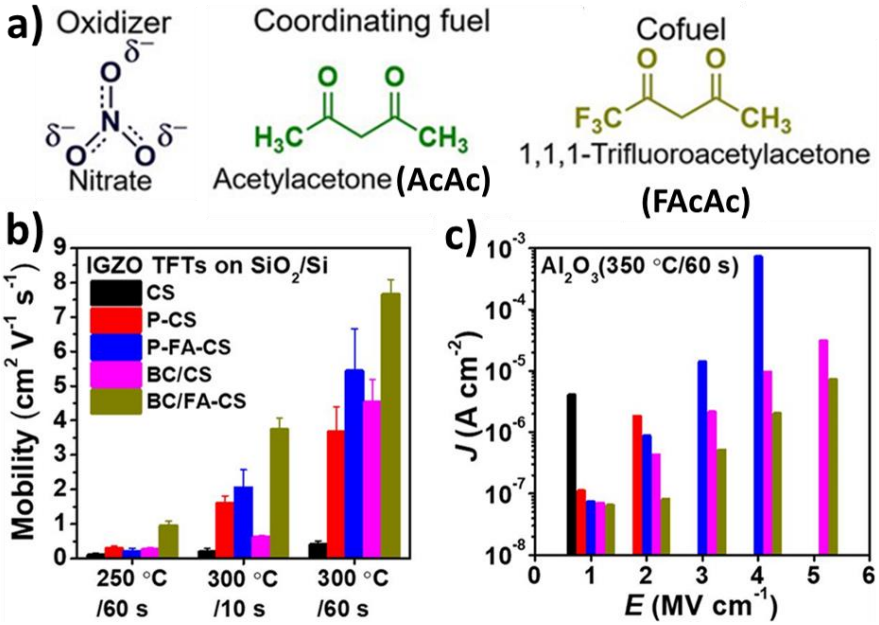

Figure 1.10. Fuel Structures and Device Performance Comparison for FAcAc Combustion Processing. a) Structures of the oxidizer (nitrate), coordinating fuel (AcAc), and cofuel (FAcAc). b) Mobility metrics for various preparations of precursor solutions. Combustion synthesis (CS), dried CS precursors (P-CS), dried fuel assisted CS (P-FA-CS), blade coating/CS (BC/CS), and blade coating with fuel-assisted CS (BC/FA-CS). c) Comparison of leakage current densities of Al_2O_3 made with different preparation methods at various electric fields. Adapted from Wang.[17]

An additional cofuel that has been integrated into combustion synthesis is 1,1,1-trifluoroacetylacetone (FAcAc) as shown in Figure 1.10 a.[17] Proton NMR (^{1}H NMR) shows that metal-AcAc$^-$ coordination occurs but metal-FAcAc$^-$ does not. Despite this, the presence of FAcAc in the precursor solution impacts AcAc$^-$ ligation. Comparing the a-IGZO TFT results for films prepared with just AcAc and those prepared with AcAc and FAcAc (10 wt. % to total weight of metal nitrates), the films with the FAcAc cofuel gave superior device metrics such as mobility, V_{th}, and I_{on}:I_{off} ratios. The study also investigated the effects of drying the combustion precursor

solutions before deposition. It was found in TGA/DSC analysis that residual solvent reduces the amount of heat generated during combustion synthesis, and the addition of FAcAc increased the amount of heat generated resulting in accelerated decomposition. The dried AcAc precursors (P-CS) resulted in superior IGZO films at significantly reduced annealing times (300 °C for 20 minutes vs. 300 °C for 10 seconds). The "wet" and dried precursor solutions produced IGZO films with a $\eta_{M\text{-}O\text{-}M}$ of 74.5% and 75.0%, respectively. IGZO films derived from dried precursor solutions containing both AcAc and FAcAc (P-FA-CS) further increased the $\eta_{M\text{-}O\text{-}M}$ to 75.9% and resulted in superior device metrics (Figure 1.10 b). The P-FA-CS preparation was also applied to an alumina dielectric. Interestingly, unlike the semiconductor films, the alumina films had some fluorine incorporation, but the P-FA-CS preparation still resulted in better dielectric performance (Figure 1.10 c).

When the study expanded from spin-coating preparation to blade coating, the P-FA-CS formulation again gave the best performance (termed BC/FA-CS), which was superior to spin-coated devices fabricated in the same manner (Figure 1.10 b). The BC/FA-CS a-IGZO and Al_2O_3 were incorporated into TFTs with impressive characteristics such as an average mobility of 18.0 ± 2.5 $cm^2\ V^{-1}\ s^{-1}$, V_{th} of 0.55 ± 0.27 V, I_{on}:I_{off} of $>4 \times 10^4$, and ΔV_{th} of 0.06 V after 4,000 seconds of bias stress. When BC/FA-CS IGZO annealed at 300 °C for one minute was used on flexible polyimide (PI) substrates with an Activink D3300 polymer dielectric and tested to a 3 mm bending radius, the mobility only decreased from 0.45 to 0.43 $cm^2\ V^{-1}\ s^{-1}$.[17]

These studies demonstrate that AcAc and NO_3^- play significant roles in the production of high-quality combustion processed films. The addition of other cofuels shows that the effects of the combustion process can be enhanced but that AcAc is still an important component.

Combustion processing is a delicate balance of the metal cations to fuel ratio that is sensitive to each new addition to the precursor solutions. Film thickness and gas evolution are also primary considerations for combustion processing parameters.

Spin-Coating Combustion Synthesis

Spin-coating was the first solution-processing method to which combustion synthesis was applied.[13] In the spin-coating process, a single layer is deposited and then annealed. These steps are then repeated to achieve the desired film thickness. The subsequent layer deposition helps to fill in any defects or pores in the previous layer resulting in the formation of thicker, denser films than a single layer deposition. The surface-to-volume ratio of the films was found to be very important to the quality of the resulting films.[13] A large surface-to-volume ratio was needed to allow for the efficient release of gaseous products to prevent the formation of porous structures and for quick heat dissipation to suppress crystallization.[13] Both of these factors limit the thickness of layers that can be spin-coated to produce good TFT performance.

Spray-Coating Combustion Synthesis

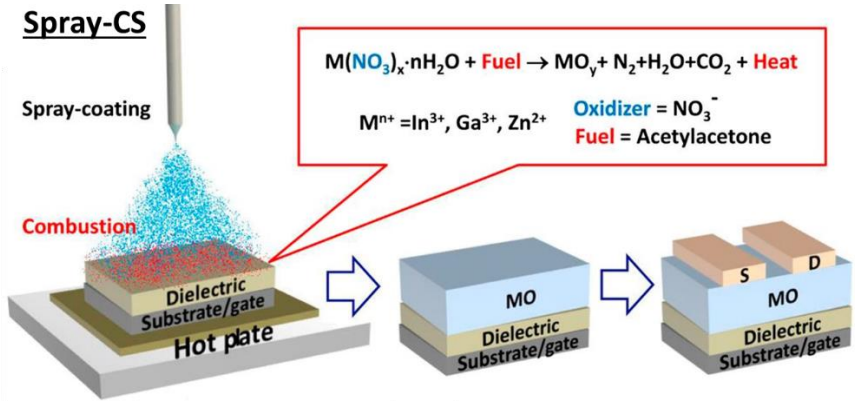

Figure 1.11. Schematic of Spray-CS TFT Fabrication. Adapted from Yu.[18]

Spray-coating involves the deposition of an aerosolized precursor solution onto a substrate while it is being annealed (Figure 1.11). Spray-coating combustion synthesis (spray-CS) has been found to minimize the porosity effects of gas evolution that require multiple layer depositions in spin-coating combustion synthesis (spin-CS), thus significantly reducing the amount of time required to achieve the same film thickness.[18] In fact, single step technologically required semiconductor thicknesses (~50 nm) via solution-processing was not possible before spray-coating.[18] Additional benefits of spray-processes are the ease of adaptability to large-area, high-throughput depositions as in roll-to-roll fabrication.[18]

Using spray-CS IGZO, films with the density, porosity, and TFT metrics such as mobility, trap densities, and bias stability from a solution-processed film approached those of a sputtered film for the first time.[18] When comparing spin-CS (fabricated by four spin-coating steps) and spray-CS (produced in a single step) 20 nm MO films, a higher $\eta_{M\text{-}O\text{-}M}$ and better TFT characteristics were seen for the spray-CS films and attributed to greater combustion efficiency.[18] X-ray reflectivity (XRR) measurements of sputtered (In:Ga:Zn 1:1:1) and spray-CS (In:Ga:Zn 1:0.11:0.29) IGZO films showed electron densities of 5.66 g cm^{-3} and 5.20 g cm^{-3}, respectively.[18] The XPS derived M-O-M content was 56% for the spray-CS IGZO films and 58% for the sputtered ones.[18] Positron annihilation spectroscopy (PAS) can quantify the porosity of films and showed that the 1:1:1 sputtered and 1:0.11:0.29 spray-CS IGZO films had a similar ~6% porosity with an average pore size of ~0.4 – 0.6 nm and a cavity density number of ~9×10^{20} cm^{-3}.[18] Capacitance versus voltage (C-V) measurements further assess the sputtered and spray-CS IGZO films' trap densities.[18] The number of C-V derived tail states were again found to be similar for the sputtered (~2.0×10^{18} cm^{-3} eV^{-1}) and spray-CS (~2.4×10^{18} cm^{-3} eV^{-1}) films.[18] The TFT metrics for the

spray-CS IGZO films are impressive with a maximum mobility of 7.6 cm^2 V^{-1} s^{-1} and an I_{on}:I_{off} ratio of ~10^8.[18] For comparison, the sputtered TFTs had an average mobility of 10.9 cm^2 V^{-1} s^{-1} and I_{on}:I_{off} of ~10^8.[18] Spray-CS has been expanded to dielectric MOs, such as Al_2O_3 and ZrO_2, as well as conducting MOs (e.g. ITO).[19] Utilizing these materials, transparent and flexible TFTs made of all spray-CS MOs were demonstrated.[19]

1.2.4 Applications

The applications of metal oxide transistors can be broadly broken down into two categories: display technologies and a number of fast moving consumer goods.[7] High resolution liquid crystal displays (LCDs) and large organic light emitting diode (OLED) TVs are now routinely manufactured from vacuum deposited metal oxide based thin-film transistors.[3, 10] IGZO TFTs were first commercialized by Sharp to form the TFT backplane for the retina LCD in the 2012 iPad.[3] An oxide TFT backplane was also incorporated into LG Display's 55 inch OLED TV in 2013.[3] By 2025, oxide TFT backplane display technology is expected to be a $87.2 billion global market.[3]

MO TFTs must meet many metrics depending on the demands of an application. High TFT mobilities enable high operating frequencies allowing for high frame rate displays.[7] OLED pixels are very sensitive to V_{th} variation that can result from bias stress effects;[5, 7] a shift of just 0.1 V can result in a 20% change in the pixel's luminosity.[7] OLEDs require a large on current (1-10 μA) for operation.[5] For OLED pixels to be on, the TFTs must produce a certain current for as long as the pixel is emitting.[5] LCDs operate by a TFT charging a pixel to the operational voltage quickly and then holding the charge until the display is changed. Overall, LCDs require lower operating

currents than OLEDs. The properties of MOs have also led to interest in and development of transparent and flexible displays.[1, 12]

Applications outside of displays include logic circuits, sensing, and wireless communication.[7, 10] To produce the complete range of logic circuits, TFT based inverters and ring oscillators are essential.[2] Simple inverters consist of two transistors while ring oscillators consist of an odd number of inverters in series.[2] Ring oscillator propagation delay is itself dependent on how quickly a TFT can operate.[2] It is hoped that the MO TFTs can play a significant role in integrated circuits for inexpensive and disposable electronics such as smart labels and radio-frequency identification tags (RFIDs).[1, 9-10, 12, 20] Photodetectors, digital X-ray imagers, and biosensors are also current applications.[3, 5, 12]

1.3 Dielectrics

Capacitors are a key component in TFTs and are just as important to device function as the semiconductor.[2] In fact the property requirements for dielectric layers are more rigorous than for semiconductors. The polarization of the dielectric induces the charges in the semiconductor, and the charges then flow at the interface of the two materials. Defects at this interface limit TFT device performance for the mobility, off current, and overall stability under bias stress.[2] These defects can occur for a number of reasons such as interfacial roughness, materials diffusion, and damage from pattering or deposition.[7] Large trap densities result in reduced stability, which is detrimental for device applications.[7]

The amount of charge accumulated in the channel (Q_{ch}) is directly proportional to the capacitance in the dielectric as shown in the following equation:

$$Q_{ch} = C_i \cdot V_G$$

The capacitance of a dielectric is defined as:

$$C_i = \varepsilon_0 \frac{k}{d}$$

where ε_0 is the permittivity of vacuum, k is the dielectric constant of the capacitor, and d is the thickness of the dielectric layer. As the above equation demonstrates, there are two ways of increasing the capacitance of a dielectric layer: 1) increase the dielectric constant and 2) decrease the thickness of the layer.[21] Increased capacitances can compensate for high trap densities resulting in reduced operating voltages and SS.[2] Silicon dioxide, the standard dielectric for decades, has a low dielectric constant (k = 3.9) and has reached the limits of its scalability. As with semiconductors, the limitations of silicon-based materials have created the need for new, unconventional dielectrics.

There are several desired characteristics for a capacitor in TFT applications: high k, low gate leakage, large breakdown strength, excellent thermal stability, and minimal trap density.[22] To utilize a capacitor in roll-to-roll fabrication, it must also be solution-processable at low temperatures compatible with flexible plastic substrates.[22] Opacity also becomes an issue for applications in transparent electronics. A significant limitation to some unconventional semiconductors, particularly organics, is the requirement of large operating voltages to achieve even relatively low mobilities.[12] Dielectrics with large capacitances can be used to achieve the desired mobilities at significantly lower operating voltages.[10, 12] To achieve low power consumption and efficient switching in electronic devices, the dielectric gate leakage must be

limited.[22] Increasing device mobility and gate capacitance are important materials-based strategies to attain better performance and boost power efficiency.[10]

Dielectric materials are classified into three categories: inorganics, organics, and hybrids, which contain both inorganic and organic materials. Inorganic materials, like metal oxides, are attractive as high *k* dielectrics. These materials also possess good durability and environmental stability. Significant drawbacks to inorganic dielectrics are the high annealing temperatures required for most solution-processing or the expensive equipment needed for vacuum deposition to achieve low leakage currents.[12] Additionally inorganic materials suffer from a trade-off between the *k* and the band gap of the materials. A reduced band gap leads to higher leakage currents and reduced breakdown strength.[2, 21] If the material is polycrystalline, the dielectric has an increased surface roughness which results in a poor dielectric interface.[2]

Organic dielectrics are inherently flexible and are typically deposited via solution-processing. Significantly organic dielectric materials can be tuned by adjusting the synthetic conditions. Organic capacitors also have low surface roughness and surface energy. High surface energy dielectrics, such as inorganics, increase the disorder in the electronic states of organic semiconductors and thus reduce the mobility. Therefore organic semiconductors generally pair better with organic dielectrics.[21] However organic dielectrics suffer from low *k*s and can only achieve higher capacitances by reducing the thickness of the layer. Thin organic layers often have poor uniformity, high off currents, and breakdown at low voltages.[21]

Hybrid organic-inorganic dielectric materials look to combine the high transparency and the electrical and environmental durability of inorganics with the flexibility and property tunability

of organics.[12] Overall the incorporation of both organic and inorganic materials into a hybrid gate dielectric can greatly improve mobility, threshold voltage, and interfacial trap density.[4]

1.3.1 Self-Assembled Nanodielectrics (SANDs) Basics

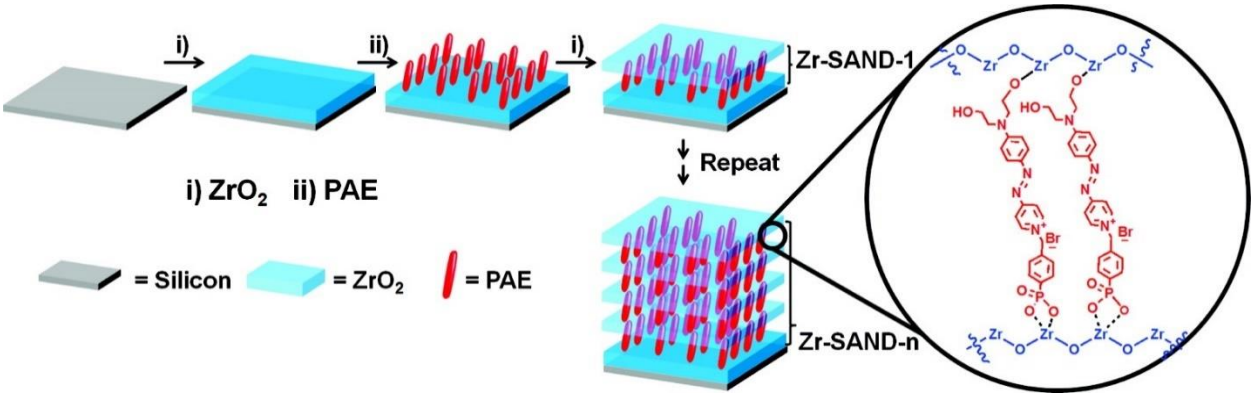

Figure 1.12. Fabrication Scheme for Zirconia-Based SAND (Zr-SAND). The iterative process is shown for four-layer Zr-SAND. Figure from Ha.[12]

Self-assembled nanodielectrics (SANDs) are hybrid dielectrics that combine the desirable characteristics of both organics and inorganics into a well-controlled and tunable multilayer structure.[12] The overall SAND structure consists of thin inorganic layers interleaved with self-assembled organic ones. An initial primer layer of oxide is deposited on top of the substrate or semiconductor depending on the device architecture. An organic layer then self-assembles onto the primer layer, and an inorganic layer is then deposited to "cap" the organic layer (Figure 1.12). The self-assembled organic layer and the capping inorganic one form a bilayer and is referred to as one-layer of SAND. The fabrication process is an iterative one that allows for additional SAND layers to be deposited as the inorganic capping layer regenerates the surface for further organic self-assembly. The advantage of successive layer deposition is that it enables defects that might be

present in one layer to be covered/minimized by additional layers. SANDs were originally developed using chlorosilane precursors.[23-24] However, these materials require inert deposition conditions that are incompatible with roll-to-roll fabrication, which is the goal of low-cost manufacturing.[12] Therefore, solution-based processes for SAND growth were developed using ZrO_x and HfO_x as the inorganics and phosphonic acid-based organics for the self-assembly.[12, 22] Impressively, solution-processed SANDs are compatible and produce superior TFT characteristics than control devices with a wide array of semiconductors such as a-IGZO,[10, 25] ZTO,[12] graphene,[11] carbon nanotubes,[26] and several organics.[12, 20, 27]

1.3.2 Organic Self-Assembly Component

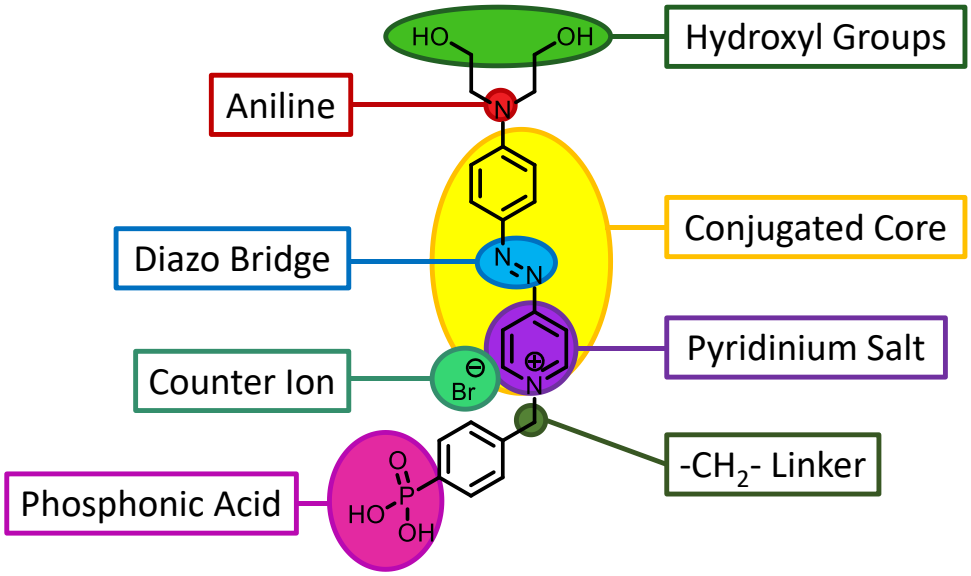

Figure 1.13. Structure of PAE. The components of the molecular structure are highlighted. Figure adapted from Dr. Riccardo Turrisi.

The organic self-assembly layer used in most solution-processed SAND is the stilbazolium derived and highly π-conjugated 4-((4-(bis(2-hydroxyethyl)amino)phenyl)diazenyl)-1-(4-

(diethoxyphosphoryl)benzyl) pyridinium bromide (PAE or Chr). PAE shares the same core structure as the self-assembly molecule in the original SiO_x based SAND but differs in the anchoring portions (phosphonic acid and hydroxyl groups).

The phosphonic acid anchoring group of PAE has a strong affinity for binding to metal oxides such as ZrO_2 and HfO_2 (Figure 1.13). The $–CH_2–$ linking group gives the PAE some steric flexibility and allows the molecule to twist in order to improve dipole alignment. The pyridinium salt acts as an electron acceptor, and the bromide counter ion balances the charge and helps to increase the overall dielectric constant. The polarizability is also increased by the stilbazolium core, which optically absorbs and thus allows for UV-Vis monitoring of the self-assembly. The diazo bridge also contributes to the polarizability of the overall molecule and provides thermostability. The aniline group acts as an electron donor for the stilbazolium core. The terminal hydroxyl groups have a lower affinity for binding to metal oxides than phosphonic acid; this results in the acid having preferential binding. The hydroxyl groups are expected to react with the capping layer providing increased structural integrity to the multilayers. The interlayer bonding between the organic and inorganic components increases the orientational stability of PAE resulting in stable capacitance and leakage characteristics.[12]

PAE has a maximum optical absorbance at 575 nm.[12] By monitoring the absorbance of a PAE monolayer, the minimum required self-assembly time was determined to be 30 minutes in a 3 mM PAE in methanol solution at 60 °C.[12] The bandgap of PAE is ~2.1 eV. PAE has a molecular length of 1.5 nm, but the thicknesses of the organic layers in SAND structures are smaller due to a molecular tilt angle of approximately 30°.[22]

1.3.3 Zr-SAND

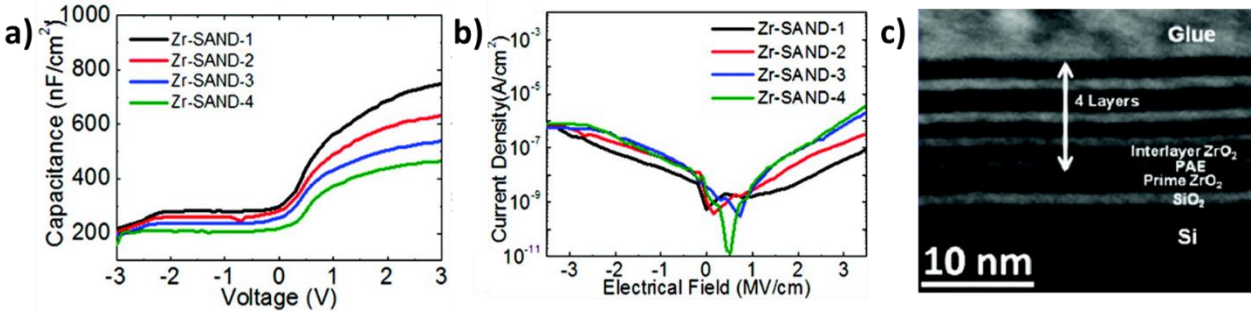

Figure 1.14. Dielectric Characterization of Zr-SAND. a) Capacitance versus voltage plots of Zr-SAND-1 – 4. b) Leakage current density versus electric field for Zr-SAND-1 – 4. c) Cross-sectional-TEM of Zr-SAND-4. Adapted from Ha.[12]

Zirconia was selected as an inorganic for solution-processed SAND due to its large band gap and high dielectric constant.[12] The absorbance of the zirconia-based SAND (Zr-SAND) at 575 nm was monitored as a function of the number of layers.[12] The absorbance increases in a linear relation as the number of layers increases, which indicates that approximately equal amounts of uniformly aligned PAE molecules self-assemble onto each layer.[12] XRR measurements of Zr-SAND multilayers show oscillating areas of high and low electron density corresponding to the ZrO_x and PAE, respectively.[12] The ZrO_x and PAE bilayers have very similar thicknesses for each layer indicating that the sequential deposition is highly uniform.[12] The ZrO_x primer layer, PAE, and ZrO_x capping layer thicknesses were ~2.1 ± 0.2 nm, 1.5 ± 0.1 nm, and 1 nm, respectively.[12] Both the alternating inorganic/organic layer structure and the layer thicknesses were also confirmed by CS-TEM (Figure 1.14 c).[12] Additionally, AFM measurements demonstrated crack and pinhole free continuous surfaces with rms roughnesses of ~0.5 nm for Zr-SAND-1 – 4 structures.[12]

Capacitance and leakage properties of Zr-SAND-1 – 4 were assessed in MIS structures.[12] The capacitances were 750 nF/cm^2 for Zr-SAND-1, 633 nF/cm^2 for Zr-SAND-2, 535 nF/cm^2 for Zr-SAND-3, and 465 nF/cm^2 for Zr-SAND-4 (Figure 1.14a).[12] The multilayer Zr-SAND structure can be modeled as capacitors in series,

$$\left(\frac{1}{C_i}\right) = \left(\frac{1}{C_{SiO_2}}\right) + \left(\frac{1}{C_{p-ZrO_2}}\right) + n \cdot \left(\frac{1}{C_{PAE}} + \frac{1}{C_{c-ZrO_2}}\right)$$

where SiO_2 is the native oxide, p-ZrO_2 is the primer layer, *n* is the number of layers, c-ZrO_2 is the capping layer, and PAE is the organic layer. The dielectric constants for the PAE and ZrO_x were determined to be ~7 and 10, respectively. The leakage current density decreased as the number of layers increased for the same applied voltage and were at least 10× lower than similarly prepared bulk ZrO_2 films (Figure 1.14 b).[12] Thermal annealing studies of Zr-SAND demonstrated that the structures are stable to at least 400 °C in ambient, which is essential for SAND integration into traditionally processed metal oxide TFTs.[12] XRR measurements demonstrated that the alternating structure of the Zr-SAND multilayers is preserved but that the thicknesses are reduced by ~20% indicative of increased densification and contraction of the ZrO_2 layers.[12] This reduction in thickness is further reflected in the capacitance increase to 650 nF/cm^2 for annealed Zr-SAND-4 (450 nF/cm^2 for the control) and a slight increase in leakage to ~6 × 10^{-6} A/cm^2 at 4 V (~3 × 10^{-6} A/cm^2).[12]

Pentacene TFTs fabricated on Zr-SAND-1 – 4 produced impressive device characteristics such as mobilities of 0.35 – 0.38 cm^2 V^{-1} s^{-1}, V_{th} of -0.5 – -0.9 V, and I_{on}:I_{off} of 10^4 – 10^5 for an operating voltage of -4 V.[12] The pentacene/300 nm SiO_2 control devices had a mobility of ~0.26 cm^2 V^{-1} s^{-1} at an operating voltage of -100 V.[12] ZTO/Zr-SAND-1 – 4 TFTs had mobilities of 3.0 –

3.5 cm^2 V^{-1} s^{-1}, threshold voltages of 0.9 – 1.1 V, and on/off current ratios of 10^5 – 10^7 at 5 V.[12] The ZTO control devices on 300 nm of SiO_2 operating at +100 V had a mobility of 1.8 cm^2 V^{-1} s^{-1}.[12]

Zr-SAND on Metal

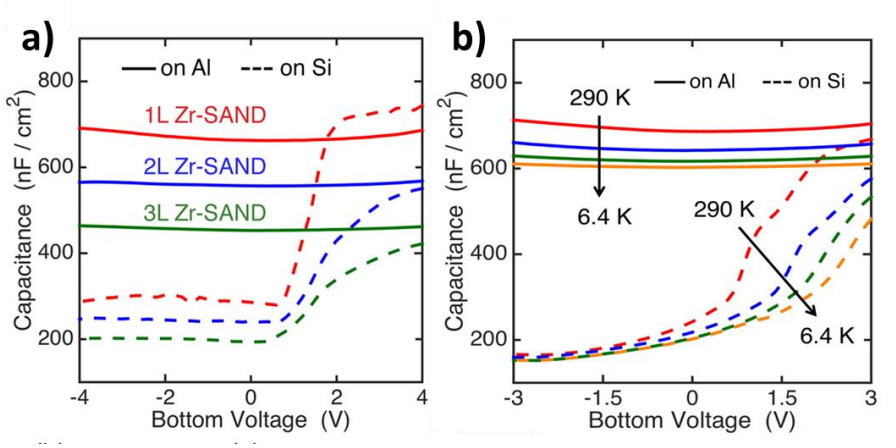

Figure 1.15. Comparison of Capacitance Behavior of Zr-SAND on Metal and on Si. a) The capacitance of Zr-SAND on metal and Si as a function of voltage. b) Capacitance of Zr-SAND on metal and Si at different temperatures. The capacitance of the Zr-SAND on metal is much more consistent than Zr-SAND on Si. Adapted from McMorrow.[4]

The dielectric properties of silicon dioxide, and thus the native oxide coated Si wafers, are dependent on gate biasing and temperature, which becomes significant for dielectric materials with higher capacitances.[4] Zr-SAND structures fabricated on template-stripped (TS) metal substrates allowed for the properties of SAND to be assessed without the limiting effects of the underlying Si substrate.[4] The TS aluminum substrates had rms roughnesses of 0.39 nm, which is significantly smoother than evaporated films alone and is important for the fabrication of smooth dielectric

surfaces (Si wafer rms roughness = 0.17 nm).[4] The resultant Zr-SAND on metal films (metal-Zr-SAND) had roughnesses between 0.55 and 0.65 nm. TEM measurements confirmed the preservation of the multilayer SAND structure.[4] The thickness of a metal-Zr-SAND-3 structure was 20.1 nm, and the thickness of each PAE/capping-ZrO_x bilayer was 3.5 nm.[4] Comparing the MIM metal-Zr-SAND with the MIS Zr-SAND on Si (Zr-SAND/Si), the metal-Zr-SAND devices' capacitance did not vary with the applied voltage while the Zr-SAND/Si devices were highly dependent on the bias (Figure 1.15 a).[4] The metal-Zr-SAND maintained impressive dielectric properties with a capacitance of ~700 nF/cm^2 and leakage current densities of <1 μA/cm^2 at -2 MV/cm. The per layer capacitance of the metal-Zr-SAND is 2675 nF/cm^2 while it is 1935 nF/cm^2 for the Zr-SAND/Si; this is again reflective of the limiting effects of the Si substrate itself in reaching full accumulation and thus preventing an accurate assessment of the capacitance behaviors of the Zr-SAND.[4] No significant differences in the leakage behavior of the Zr-SAND on metal and the Zr-SAND on Si were observed.[4] However significant differences in the temperature dependent (290 – 6.4 Kelvin) C-V measurement were seen (Figure 1.15 b).[4] As the temperature decreased the capacitance decreased for all samples, but the change in the metal-Zr-SAND (15% at 3 V) was significantly less than that of the Zr-SAND/Si (47% at 3 V).[4] Importantly, the development of SAND on metal allows for future detailed experiments to investigate both the SAND itself and the transport in semiconductors that might be deposited onto it.[4]

Zr-SAND Radiation Studies

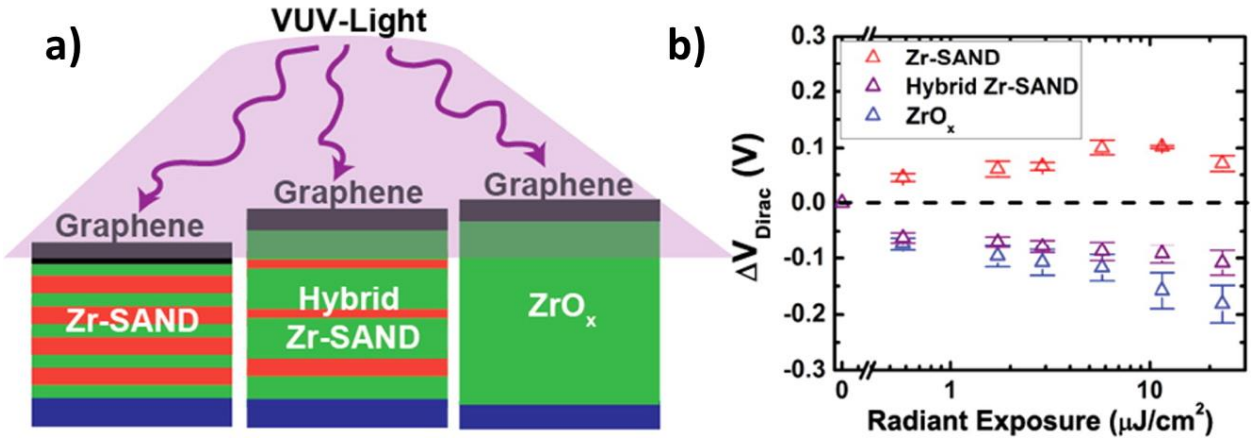

Figure 1.16. Zr-SAND Structures and Radiation Response. a) Graphic representation of the three different dielectric samples studied for radiation response. b) Radiation response by sample. The response of the hybrid Zr-SAND falls between that of the Zr-SAND and ZrO_x demonstrating the structure's tunability.

The importance of the tunability of SAND structures was demonstrated by the use of Zr-SAND in graphene based TFTs for radiation response studies.[11] The stability of electronics on exposure to radiation is important for applications in satellite technologies that function in low Earth orbit.[11] The TFT responses were measured as a function of total ionizing dose (TID) generated by vacuum ultraviolet (VUV) radiation.[11] Evaluation of the TFTs results indicated that the primary source of device degradation upon radiation exposure came from changes in the Zr-SAND.[11] The negative charge density in the Zr-SAND increased upon exposure to VUV, but a ZrO_2 only dielectric had an increase in both hole and electron charge density.[11] This indicates that the organic PAE layers in Zr-SAND only experience an increase in negative charge density, which compensates for the hole trapping of the ZrO_x.[11] To further confirm the competing charge trapping

mechanisms of the PAE and ZrO_x layers, the thickness of the ZrO_x was varied to determine if the radiation response could be adjusted (Figure 1.16 a).[11] The radiation response of the hybrid Zr-SAND devices with increased ZrO_x layer thicknesses fall between that of the regular Zr-SAND and the pure ZrO_x devices, indicating that radiation response can indeed be tuned (Figure 1.16 b).[11]

Inverted SAND

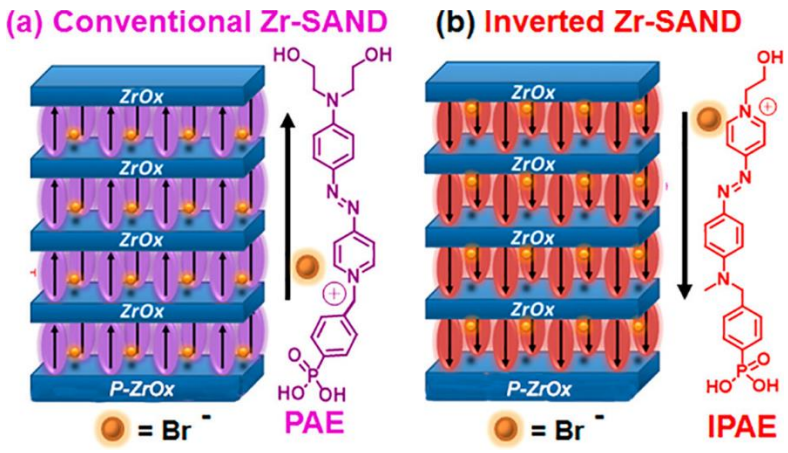

Figure 1.17. Zr-SAND and IZr-SAND Four-Layer Structures. a) Zr-SAND-4 with the structure of PAE and the direction of the dipole moment indicated. b) IZr-SAND-4 with the structure of IPAE and dipole moment direction. Figure from Wang.[27]

The importance of the organic layer component in SANDs has been established by the superior TFT performance afforded by SAND dielectrics versus comparable inorganic ones[22] and by the PAE's unique radiation response in SAND based TFTs.[11] To better understand the effects of PAE on Zr-SAND function, a new phosphonic acid based self-assembly molecule with the opposite dipole, IPAE, was developed (Figure 1.17).[27] PAE and IPAE are both optically absorbing but have different maximum absorbance wavelengths (λ_{max}), which are 575 nm and 547 nm respectively.[27] UV-Vis measurements of the Zr-SAND structures incorporating IPAE instead of

PAE (IZr-SAND) indicate a linear increase in the absorbance as the number of layers increase, which demonstrates consistent IPAE self-assembly for each organic layer. The alternating high and low electron density of the inorganic and organic multilayer structure were confirmed by XRR. Kelvin probe measurements were used to assess the surface dipole of PAE and IPAE by determining the contact potential difference (CPD) between gold (as the reference surface) and the sample. CPD values for primer ZrO_x, PAE/primer ZrO_x and IPAE/primer ZrO_x samples were ~ -770, -983, and -463 meV respectively. These results are in accordance with the expected dipole orientations of the organic constitutents.[27]

The capacitance for IZr-SAND-1 – 4 (770 – 503 nF/cm^2) is slightly higher than that of Zr-SAND-1 – 4 (750 – 465 nF/cm^2) and is attributed to the small differences in the PAE and IPAE structures and opposite polarization orientations. The different orientations of the dipoles are reflected in the different dC/dV values for Zr-SAND and IZ-SAND, where the IPAE is oriented with the applied electric field. Additionally, the onset of accumulation was more positive for Zr-SAND-1 – 4 (-100 to 250 mV) than IZr-SAND-1 – 4 (-400 to 300 mV). C-f measurements show the IZr-SAND has greater capacitance stability over a larger frequency range (1×10^5 Hz) than Zr-SAND (3×10^4 Hz). However, IZr-SAND and Zr-SAND exhibit similar leakage currents of ~1 – 2×10^{-6} A/cm^2 at 3 V.

For many applications, the fine tuning of TFT metrics is key.[27] It has long been established that semiconductors, particularly organic ones, are sensitive to the electronic environment of the semiconductor/dielectric interface. Significant threshold voltage shifts have been achieved in OTFTs with the use of SAMs of different polarity and terminal functional groups.[21] IZr-SAND and Zr-SAND TFTs were fabricated with pentacene and 1,2,3,4,8,9,10,11,15,16,17,18,22,23,-

24,25-hexadecafluoro-29*H*,31*H*-phthalocyanine (F_{16}PcCu). The devices had similar mobilities. A negative V_{on}/V_{th} shift of -50 to -700 mV was observed for both semiconductors when going from Zr-SAND to IZr-SAND. Kelvin probe measurements on IZr-SAND and Zr-SAND are almost identical to the ZrO_x priming layer indicating the ZrO_x capping layer moderates the CPD.

To better evaluate the effects of the organic layers, Zr-SAND and IZr-SAND were capped with Me_3Si- instead of ZrO_x to produce cZr-SAND and cIZr-SAND. The difference in the onset of accumulation for capacitance measurements of cZr-SAND (-0.09 V) and cIZr-SAND (0.16 V) were more pronounced. For the pentacene and F_{16}PcCu cZr-SAND and cIZr-SAND devices, the V_{on}/V_{th} shifts become much more significant. For the pentacene transistors going from cZr-SAND to cIZr-SAND resulted in a V_{on} shift of -1500 mV and a V_{th} shift of -650 mV. Similarly, for the F_{16}PcCu TFT changing from cZr-SAND to cIZr-SAND resulted in a V_{on} shift of -1300 mV and a V_{th} shift of -700 mV. The V_{on}/V_{th} shifts are consistent with the different dipole orientations of IPAE and PAE. The molecular dipole moment along the molecular long axis is abbreviated as $P_{\perp}$. Using the change in V_{on} for IZr-SAND and Zr-SAND, the $P_{\perp}$ was estimated to be 2.00 D for the IPAE layers and -1.45 D for the PAE layers. These results are in accordance with the $P_{\perp}$ values for IPAE (0.70 D) and PAE (-3.04 D) estimated from DFT computations and long-period X-ray standing wave experiments.[27] Thus it was demonstrated that the capacitance properties of SAND and V_{th}/V_{on} of organic transistors can be tuned using the dipole moment of the organic layer component.[27]

Printed Zr-SAND (PSAND)

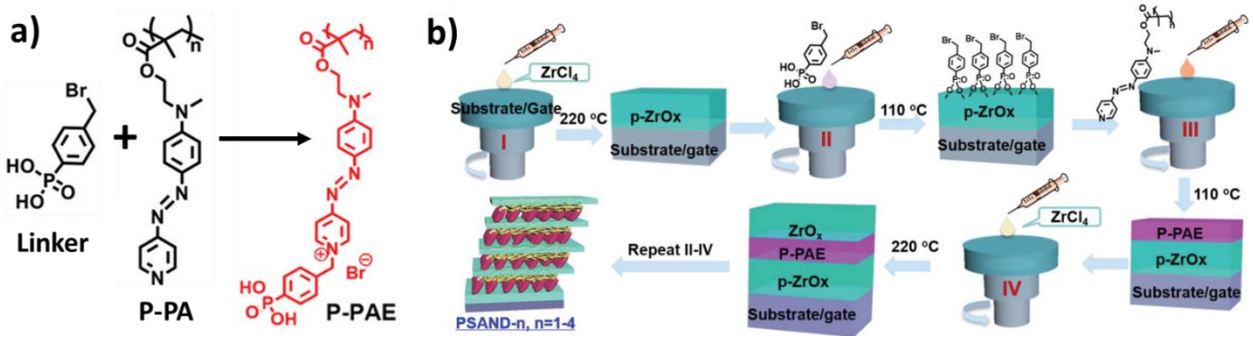

Figure 1.18. P-PAE Structure and PSAND Fabrication Scheme. a) The structures of the linker, P-PA, and P-PAE. b) PSAND fabrication scheme. The processing temperature is indicated for each step. Adapted from Chen.[20]

While significant progress in printed devices for use on flexible plastic substrates has been made, most printed TFTs require undesirably large operating voltages as a result of limitations in the processing quality of the semiconductor and dielectric.[20] Due to the time constraints of the traditional PAE layer self-assembly, a modified PAE was developed, P-PAE, to be implemented in a spin-coating deposition process.[20] P-PAE possesses a polymeric backbone and a stilbazolium based phosphonic acid functionalized PAE structure for self-assembly (Figure 1.18 a).[20] The new organic layer component was deposited in a two-step sequence. First a self-assembled linker molecule is deposited onto the ZrO_x surface. A stilbazole functionalized polymer (P-PA) then reacts with the linker to form P-PAE *in situ*.[20] Both components are deposited via spin-coating followed by annealing at 110 °C for 20 minutes (Figure 1.18 b).[20] TGA studies demonstrate that the decomposition temperatures for the linker and P-PA are 267 and 262 °C respectively, which are above the typical processing temperatures for SANDs.[20] P-PA on glass has a maximum

absorption at 430 nm. When P-PA reacts with the linker, the λ_{max} shifts to 450 nm, which is much higher than PAE (λ_{max} = 575 nm). From the differences in λ_{max}, it was determined that only ~12-13% of the P-PA reacts with the linker on the ZrO_x surface. Importantly the absorption at 450 nm increases linearly with the deposition of additional layers indicating that P-PAE deposition is essentially uniform for all layers, as seen in other SAND iterations.[20] XRR confirmed the expected oscillating electron density in the multilayer organic/inorganic structure.[20] AFM demonstrated that the roughnesses for all PSAND-1 – 4 structures were ~0.20 nm.[20]

The capacitance and leakage properties of the PSAND dielectric, evaluated in MIS structures, are excellent with capacitances ranging from 558 nF/cm^2 for PSAND-1 to 339 nF/cm^2 for PSAND-4 and leakage current densities of ~10^{-6} A/cm^2 at 2 MV/cm. The PSAND structures also have impressive breakdown strengths (10.52 MV/cm to 8.57 MV/cm). The *k* of the P-PAE layer is ~6 which is consistent with the lower amounts of fully reacted linker and P-PA.[20] The PSAND dielectrics were capped with HMDS before implementation into TFTs with the organic semiconductors pentacene, F_{16}PcCu, N,N'-1*H*,1*H*-perfluorobutyl dicyanoperylenecarboxydiimide (PDIF-CN_2), and diketopyrrolopyrrole-dithienyl-thieno[3,2-*b*] thiophene (DPP-DTT), a polymer. Pentacene and F_{16}PcCu were vapor deposited while DPP-DTT and PDIF-CN_2 were solution deposited. The TFT results were comparable to previous TFTs made with Zr-SAND which demonstrates the quality of the new PSAND. Furthermore DPP-DTT/HMDS coated PSAND-4 TFT were fabricated on flexible polyimide (PI) substrates. The TFTs had a mobility of 0.18 cm^2 V^{-1} s^{-1}, a V_{th} of -0.21 V, and an I_{on}:I_{off} ratio of 10^3 which were similar to the devices fabricated on Si substrates. The TFTs maintain excellent device performance after bending to 2 mm for 1000 times (μ = ~0.2 cm^2 V^{-1} s^{-1} and V_{th} ~ 0.7 V). Importantly PSAND-1 was also deposited by printable

blade-coating. The structure was confirmed by XRR (~6.1 nm), and the surface roughness was 0.12 nm as determined by AFM. The capacitance was 497 nF/cm^2, and the leakage was ~10^{-6} A/cm^2 at 2 MV/cm. DPP-DTT transistors were then fabricated on the blade-coated PSAND by both spin-coating and blade-coating, which resulted in very similar performance (μ = 0.11 cm^2 V^{-1} s^{-1} for spin-coating and μ = 0.10 cm^2 V^{-1} s^{-1} for blade coating).[20] PSAND is the first demonstration of the SAND dielectric family utilizing printing processing methods and shows excellent mechanical flexibility properties as needed for the next generations of unconventional electronics.

1.3.4 Hf-SAND

The use of hafnia as the metal oxide in the SAND structure, as opposed to ZrO_x, was motivated by its higher dielectric constant and different surface chemistry.[22] Specifically phosphonic acids are known to have greater affinity for hafnia surfaces than zirconia ones, which significantly affects surface coverage.[22] With the exception of the metal chloride used to make the precursor solutions, Hf-SAND is fabricated in the same manner as Zr-SAND.

Hf-SAND-1 – 4 layer structures were fabricated. AFM showed that the Hf-SAND films were smooth (0.13 – 0.17 nm), which is essential for semiconductor deposition in BG TFTs.[22] The XRR demonstrated the expected oscillations of high and low electron density for the inorganic and organic layers respectively.[22] The HfO_x primer layer, PAE organic layer, and capping HfO_x layer are 2.2 nm, 1.3 nm, and 1.2 nm thick respectively.[22] The layered structure and layer thicknesses were also confirmed by CS-TEM.[22] Hf-SAND structures were also characterized by XPS; the first time this technique was applied to SAND.[22] Signals from hafnium, oxygen, and carbon were detected but nitrogen, bromine, and phosphorous were not due to the coverage of the HfO_x capping

layer and their limited concentrations.[22] The exact breakdown and quantification of the O 1s peak is impossible due to the extremely thin HfO_x layer's abundant surface hydroxyl groups.[22] However the O 1s peaks were determined to be qualitatively similar between Hf-SAND samples annealed at 150 °C and 300 °C and dominated by the HfO_x peak indicating that well condensed Hf-O-Hf networks form even at the lower processing temperature.[22] This was confirmed by the Si normalized electron density of the HfO_x layers matching that of bulk crystal HfO_2.[22] Importantly XPS did not detect any chloride from the precursor materials present in the films, which is again indicative of the high quality of the HfO_x films.[22]

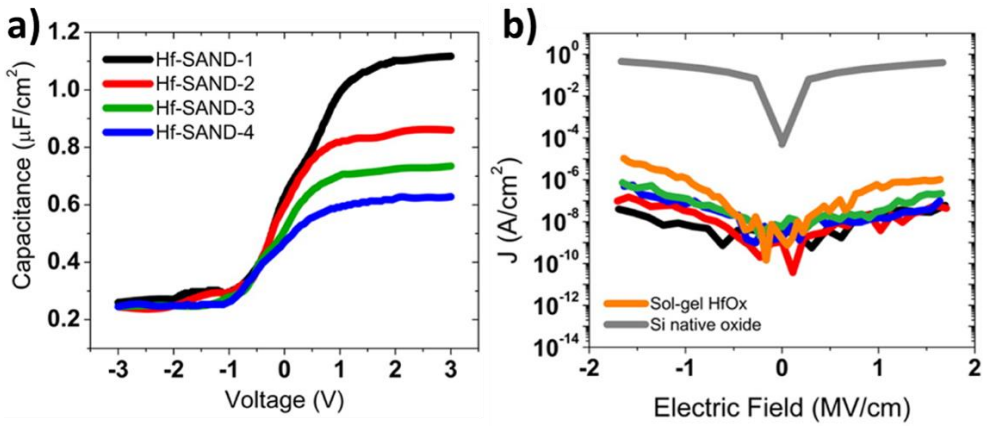

Figure 1.19. Dielectric Characterization of Hf-SAND-1 – 4. a) Representative C-V plots for Hf-SAND-1 – 4. b) Leakage current density versus electric field for Hf-SAND-1 – 4. Adapted from Everaets.[22]

The Hf-SAND-1 – 4 layer structures had impressive capacitance and leakage properties (Figure 1.19). The capacitances were 1100 nF/cm^2, 850 nF/cm^2, 720 nF/cm^2, and 610 nF/cm^2 for Hf-SAND-1, -2, -3, and -4 layer structures respectively.[22] The k_{eff} (overall dielectric constant) for the Hf-SAND stacks increases as the number of layer increases indicating that the PAE layer has

a higher dielectric constant (k = 15) than the HfO_x (k = 13).[22] This PAE layer k is significantly higher than that of PAE layers in Zr-SAND (k = 7).[22] XRF measurements determined that the PAE surface coverage for Hf-SAND was 30 ± 10% greater than that of Zr-SAND helping to explain the difference in the PAE layer dielectric constants.[22] Additionally, the Hf-SAND hafnia layers' k of 13 is higher than that of the Zr-SAND zirconia k of 10.[12, 22] The Hf-SAND dielectrics showed excellent leakage performance with leakage current densities ranging from 3.9×10^{-8} to 7.2×10^{-7} A/cm^2 at -2 MV/cm (Figure 1.19 b).[22] The Hf-SAND also had impressive average breakdown fields of ~5.5 MV/cm, which increased to almost 8 MV/cm when the films were annealed at 250 °C.[22] Hf-SAND was also demonstrated to be stable during annealing at 400 °C in ambient for thirty minutes.[22] Hf-SAND-1 was incorporated into single-walled carbon nanotubes (SWCNT) TFTs.[22] These devices had metrics comparable to the best reported in the literature showing the excellent compatibility of Hf-SAND with carbon nanotubes.[22]

Printed Combustion Processed a-IGZO/Hf-SAND TFTs

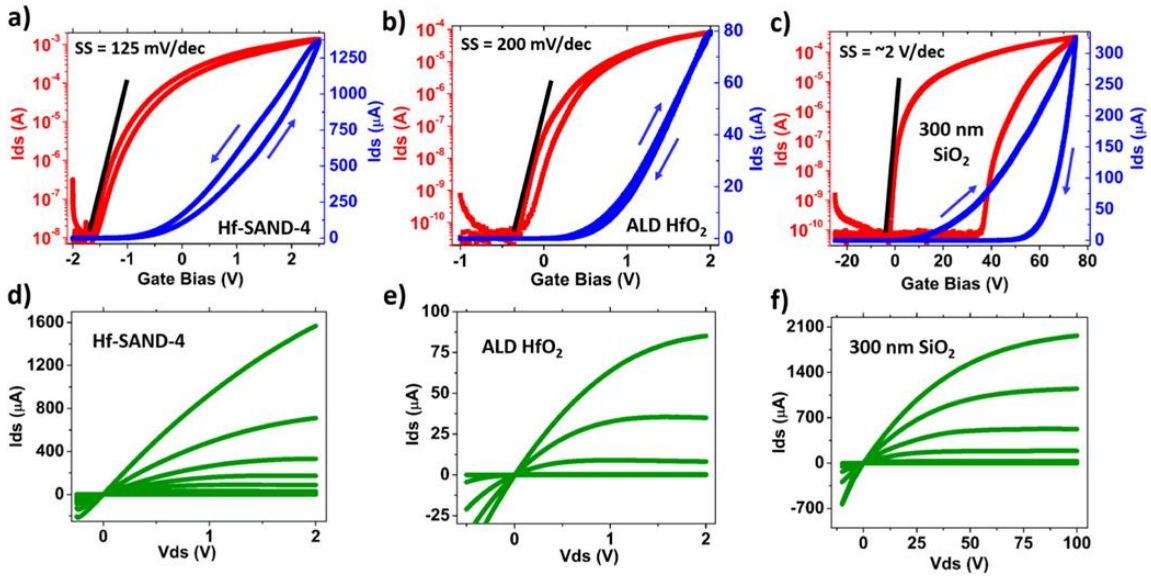

Figure 1.20. Representative Transfer and Output Plots for Inkjet-Printed Combustion Processed a-IGZO TFTs on Various Dielectrics. Transfer and output plots on Hf-SAND-4 (a and d), ALD HfO_2 (b and e), and 300 nm SiO_2 (c and f). Figure from Everaerts.[10]

Inkjet-printed combustion processed a-IGZO was deposited in five layers with annealing at 300 °C for 20 minutes in ambient conditions. The a-IGZO deposition had minimal densification effects on the underlying Hf-SAND.[10] Impressively the a-IGZO deposited on the Hf-SAND and SiO_2 had the same rms roughness (~0.2 nm).[10] a-IGZO/Hf-SAND TFTs produced excellent device characteristics such as an average mobility of 20.6 ± 4.3 $cm^2\ V^{-1}\ s^{-1}$ (μ_{MAX} = 50 $cm^2\ V^{-1}\ s^{-1}$) at an operating voltage of 2 V, an on/off current ratio of 10^7, and a SS of 125 mV/dec.[10] Comparable devices using SiO_2 or ALD-HfO_2 as the dielectrics had average mobilities of 2.9 ± 2.1 and 4.0 ± 2.1 $cm^2\ V^{-1}\ s^{-1}$ respectively (Figure 1.20).[10] The ALD-HfO_2 had a capacitance of 590 nF/cm^2, which is similar to that of Hf-SAND-4 (605 ± 30 nF/cm^2); therefor the ALD-HfO_2 TFTs served as

excellent controls.[10] The comparisons of the a-IGZO/ALD-HfO_2 and a-IGZO/Hf-SAND-4 devices indicates that the Hf-SAND produces device enhancements, likely due to the effects of the PAE layers, beyond the capacitance values.[10] It should be noted that while the a-IGZO/Hf-SAND devices have minimal hysteresis, it is in the clockwise direction while IGZO devices typically have anticlockwise hysteresis,[28] which is another indication of unique interactions with the Hf-SAND dielectric.

Chapter 2

Effects of the Organic Layer Structure and Arrangement in Self-Assembled Nanodielectrics for Organic Transistors

2.1 Background

Organic electronics have attracted significant attention in both research and manufacturing for decades.[1-4] This is due to the potential for solution-processing the entire organic device architecture via high throughput printing, which eliminates the need for photolithography, significantly reduces production times, and lowers cost.[4-5] Additionally, organic devices allow for low temperature processing, when compared to traditional silicon and most conventional metal oxide based electronics, onto plastic substrates, therefore, enabling flexible and even stretchable devices.[6] The applications for these high throughput electronics include wearable electronics,[7-8] radio frequency identification tags (RFID),[3, 5] and a variety of (bio)sensors.[3, 9-11]

Despite the many promising qualities of organic semiconductors, there are several drawbacks. Compared to metal oxide semiconductors, organic semiconductors have significantly lower field-effect mobilities and drain currents, thus resulting in higher operating voltages.[3] Since the turn-on voltage (V_{on}) is the voltage at which a device enters the on state,[12] a lower V_{on} or threshold voltage (V_{th}) results in lower operating voltages and reduced energy consumption.[3] High operating voltages are detrimental to portable electronics that operate on battery power.[3, 13] The drain current (I_{DS}) and the mobility of a TFT in saturation (μ_{SAT}) are given as:

$$I_{DS\,SAT} = \frac{\mu_{SAT} W C_i}{2L}(V_G - V_{th})^2 \qquad \text{(Eq. 1)}$$

$$\mu_{SAT} = \frac{2L}{WC_i}\left(\frac{\partial\sqrt{I_{DS\,SAT}}}{\partial V_G}\right)^2 \qquad \text{(Eq. 2)}$$

where C_i is the capacitance per unit area of the gate dielectric, *W* is the channel width, *L* is the channel length, and V_G is the voltage applied between the source and the gate.[14] From Equations

1 and 2, it is clear that the drain current and, thus, the mobility is dependent on the C_i, so increasing the capacitance also increases the drain current. The C_i of the dielectric is given by:

$$C_i = \varepsilon_0 \frac{k}{d} \qquad \text{(Eq. 3)}$$

where ε_0 is the permittivity of vacuum, k is the dielectric constant, and d is the thickness of the dielectric layer.[15] To increase the capacitance, k must be increased and/or the dielectric thickness must be decreased. Since the traditionally used silicon dioxide has a relatively low dielectric constant (k = 3.9) and has reached the limits of its device scaling, unconventional dielectrics must be employed to enhance drain currents and lower turn-on voltages to utilize the promising properties of organic semiconductors.[16]

The search for unconventional dielectrics to enable low voltage organic devices has included different classes of dielectrics such as organics,[8, 17] inorganics,[18] and hybrids.[16] Organic dielectrics provide low processing temperatures and mechanical flexibility but suffer from low *k*s, which as shown in Equations 1, 2, and 3, is detrimental to low power operation.[3] Inorganic dielectrics offer high dielectric constants and good environmental stability; although they typically require high temperature processing incompatible with the plastic substrates that allow for the mechanical flexibility of organic semiconductors to be utilized.[3, 19] The compatibility of organic semiconductors with inorganic dielectrics is also limited as high *k* dielectrics have been found to increase the disorder in the electronic states of the semiconductor, resulting in decreased mobility.[1, 16, 20] Hybrid dielectrics look to combine the benefits of both organic and inorganic materials while minimizing the disadvantages, particularly for organic semiconductors.[13, 16]

One such hybrid organic-inorganic dielectric is self-assembled nanodielectrics (SANDs), which are composed of alternating inorganic layers such as ZrO_x and self-assembled high *k* organic layers. SANDs are processed at low temperatures (≤200 °C) meaning they are compatible with inexpensive flexible plastic substrates.[21] Additionally, the SAND structure allows for immense amounts of tailorability in both the inorganic and organic layer components. The inorganic layers have been tailored in terms of both thickness[22] and material (e.g. SiO_x, Al_2O_x, ZrO_x, HfO_x).[15, 23-25] Variations of the self-assembled phosphonic acid anchored stilbazolium salt derived organic layers have also been developed.[21, 26] In addition to the valuable materials and thickness tunability, SANDs provide high capacitance, lower leakage currents compared to similar solution-processed all inorganic films, mechanical flexibility, and radiation hardness.[15, 21-23, 27] Recently SANDs have been developed that can be printed[21] and demonstrated in more complex top-gate TFT structures.[28] SANDs are compatible with a wide range of semiconductors such as a-IGZO,[27] graphene,[22] carbon nanotubes,[25] and a variety of organics.[15, 26] SAND based TFTs have been found to give superior device metrics compared to similar all inorganic dielectric TFTs.[27] The superiority of SAND TFTs has especially been attributed to the effects of the stilbazolium derived organic layer's high polarizability and built-in dipole moment.[27]

Recently the effects of the highly polarizable self-assembled organic layer have been investigated by using two different phosphonic acid based organic molecules of opposite dipoles, which resulted in shifts in both the V_{on} and V_{th} in TFTs.[26] In this work, an alkyl chain phosphonic acid based self-assembly molecule (**Alk**) is developed to further understand the workings of the organic layers within the overall SAND structure. **Alk** has limited polarizability and no built-in dipole unlike the previously used organic molecules (PAE or **Chr**). By changing the arrangement

of **Alk** and **Chr** layers within the SAND structure, the effects of an organic layer's built-in dipole, or lack thereof, on the device metrics of both capacitors and pentacene based TFTs are studied. The dielectric structures with differing arrangements of **Alk** and **Chr** show exceptionally similar capacitance and leakage values, but the dipole of the **Chr** layers has a significant impact on the dielectric breakdown strength and indicates that coupling between adjacent **Chr** layers occurs, enhancing the effects. The zirconia SAND (Zr-SAND) based pentacene transistors reveal that the dipole of the organic layer closest to the channel impacts the turn-on voltage, threshold voltage, and on current to off current ratio. The TFT results also suggest coupling between adjacent **Chr** layers. Overall, this study provides further information on the tunability of the unique SAND structure for specific operating requirements.

2.2 Experimental Section

2.2.1 SAND Film Fabrication

The zirconium oxide precursor solutions were prepared using zirconium (IV) chloride (99.5% Aldrich) as received. A stock 0.1 M $ZrCl_4$ solution was made with 93.8 g in 4 mL of absolute ethanol. The solution was stirred at room temperature for five minutes before the addition of 264 µl nitric acid at which point the solution was heated to 50 °C and stirred for three hours. The solution was then aged overnight at room temperature. The stock 0.1 M ZrO_x solution was diluted with absolute ethanol to prepare a priming solution (0.02 M ZrO_x) and a capping solution (0.01 M ZrO_x) approximately one hour before use. A HEPA filtered laminar flow clean hood containing plasma cleaning, spin-coating, annealing, and self-assembly apparatuses was used for the SAND deposition. Highly n-doped Si substrates (WRS Materials) were sonicated in acetone,

hexanes, and ethanol for 10 minutes each and then air plasma cleaned on high for five minutes (400-500 mTorr) before use. During the spin-coating procedure, all of the ZrO_x solutions (both priming and capping) were passed through a 0.2 μm Teflon syringe filter. The ZrO_x primer layer was made by spin coating the 0.02 M ZrO_x solution onto the Si substrates at 5000 rpm for 30 seconds, followed by annealing at 200 °C for 20 mins.

The 4-[[4-[bis(2-hydroxyethyl)amino]phenyl]diazenyl]-1-[4-(diethoxyphosphoryl) benzyl] pyridinium bromide (PAE or **Chr**) and 11-hydroxyundecylphosphonic acid (PAA or **Alk**) were synthesized as previously published.[15,29] A 3 mM solution of PAE in methanol and a separate 3 mM solution of PAA in methanol were prepared for the organic layer self-assembly. The 3 mM solutions were heated to 60 °C for the entirety of the self-assembly. The ZrO_x primed substrates were then submerged in the PAE or the PAA solution depending on the desired structure for one hour as the self-assembly took place. The substrates were then sonicated in methanol for 5 minutes and then individually cleaned in fresh methanol for 1 minute to remove any excess organics. A capping layer was spin-coated onto the organic layer using the 0.01 M ZrO_x solution at 5000 rpm for 30 seconds and then annealed at 200 °C for 20 minutes (the same manner as the primer layer). The oxide and self-assembly steps were repeated to achieve the desired three-layer structures.

2.2.2 SAND Film Characterization

X-ray reflectivity (XRR) measurements were performed on a 9 kW Rigaku Smartlab Workstation. X-rays were generated from the Cu rotating anode (X-ray wavelength is 1.542 Å) and collimated to produce a monochromated X-ray beam with dimension 0.1 × 5 mm and flux ~3 × 10^8 cps at the sample surface. The XRR data was modeled and fitted using the Motofit package[30] to obtain the electron-density profile, which contains information such as the thickness, electron

density, and interfacial roughness of each layer. Atomic force microscopy (AFM) measurements were taken using a Burker Dimension FastScan AFM.

2.2.3 Electrical Characterization of SAND Films

The metal-insulator-semiconductor (MIS) capacitors were made from the various three-layer Zr-SAND structures on Si substrates. Thermal evaporation (Denton) through shadow masks produced the top gold contacts (200 × 200 μm). The MIS electrical measurements were performed using an Agilent B1500A semiconductor parameter analyzer under ambient conditions. For the capacitance vs voltage (C-V) and the leakage current density vs voltage (J-V) curves, a beryllium-copper alloy probe (SE-BC, Signatone) served as the anode and a flexible tungsten whisker probe (SE-SM, Signatone) served as the cathode. The C-V curves were taken at 10 kHz.

2.2.4 Pentacene Transistor Device Fabrication, Electrical Measurements, and Film Characterization

Pentacene (P5, 99%, Sigma-Aldrich) was sublimated twice before use in a three-zone sublimator (290, 275, 230 °C).Using the three-layer Zr-SAND samples produced as previously described, pentacene was thermally evaporated (Denton, 50 nm, 0.1 Å s^{-1}) onto the dielectric substrates (kept at 25 °C). Gold was thermally evaporated (Denton, 40 nm) through shadow masks for the source and drain contacts (W = 1 mm, L = 50 μm). An Agilent B1500A semiconductor parameter analyzer was used for the transfer and output measurements under ambient conditions. To extract the saturation regime carrier mobilities (μ_{SAT}), the standard field-effect transistor model was used. The pentacene films were assessed by AFM using a Burker Dimension FastScan AFM.

2.3 Results and Discussion

In the following sections, we first explain the nomenclature and growth of the various Zr-SAND dielectric structures used in this work. The self-assembly of **Alk** onto ZrO_x is confirmed with contact angle studies, and the morphology is accessed with AFM. The Zr-SAND dielectric structures with differing organic layers are evaluated morphologically by AFM, structurally by XRR, and electrically by both capacitance and leakage measurements. Organic TFTs (OTFTs) are fabricated using pentacene as the semiconductor, and the transistor results and pentacene crystallite morphology are discussed.

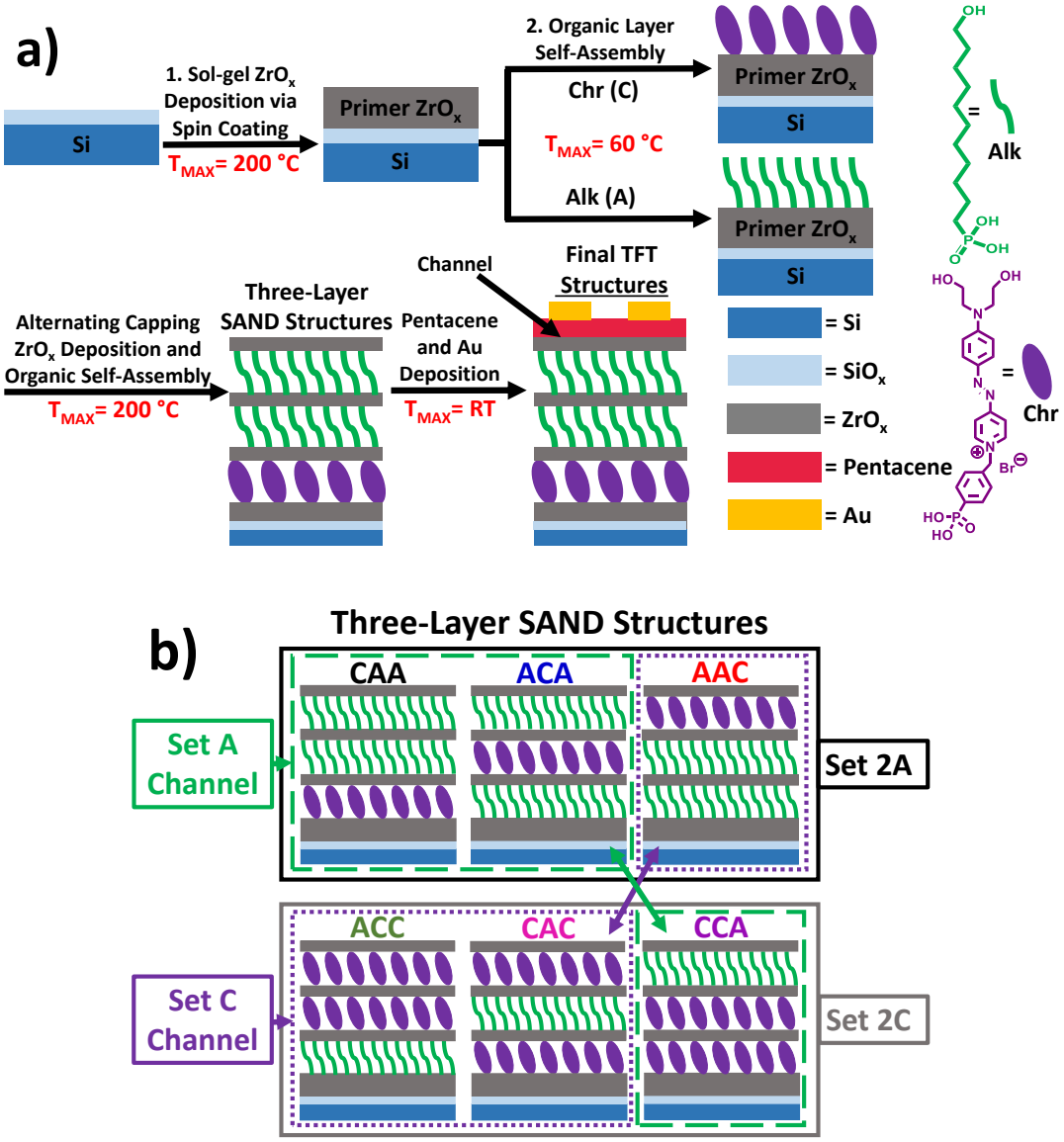

Figure 2.1. Fabrication and Naming of Zr-SAND Samples. (a) Fabrication scheme for a representative Zr-SAND structure (CAA) and the corresponding pentacene TFT. The processing temperature of each step is indicated. (b) The six different Zr-SAND structures used in this study with the groupings referred to in the analysis. **Chr** layers are represented by the purple ovals and **Alk** layers by the wavy green lines. The samples are named based on the layer closest to the substrate and then moving up through the organic layers to the one closest to what would be the channel in a bottom-gate TFT structure. The components are not drawn to scale.

2.3.1 Zr-SAND Film Growth

Figure 2.1 shows the fabrication scheme for the various Zr-SAND structures investigated in this work and the corresponding pentacene TFTs with further details reported in the Experimental Section. Briefly, the initial ZrO_x layer, referred to as the primer layer, was spin-coated onto clean Si substrates and annealed at 200 °C. There are two different organic self-assembly layers used in the Zr-SAND structures for this study. The stilbazolium based organic constituent, 4-[[4-[bis(2-hydroxyehtyl)amino]phenyl]diazinyl]-1-[4-(diethoxyphos-phoryl) benzyl pyridinium (PAE), was used exclusively as the organic layer in previous solution based SAND iterations[15, 24, 31] and will be referred to as the chromophore (**Chr**) in text or **C** in figures and tables. The hydrocarbon based organic molecule, 11-hydroxyundecylphosphonic acid, will be referred to as **Alk** and **A** in text or figures and tables, respectively. Either **Chr** or **Alk** were self-assembled onto the primer layer depending on the desired Zr-SAND structure. The self-assembly layers were then capped with a thin layer of ZrO_x, which produces an organic/inorganic bilayer. Each bilayer is considered one-layer of the SAND structure. The self-assembly and zirconia capping steps were repeated two more times to produce three-layer Zr-SAND structures (Zr-SAND-3).

There are six different SAND samples with varying arrangements of organic layers used in this study (Figure 2.1b). The samples are named based on the layer closest to the substrate (Si), and then moving up through the organic layers to the one closest to what would be the channel in a bottom-gate TFT structure. For example, a sample that has a **Chr** layer closest to the substrate, an **Alk** layer as the second organic layer, and an **Alk** layer closest to the channel is named CAA. The samples are further grouped in four clusters of three, with each sample belonging to two

separate groups. Those with two **Alk** layers and one **Chr** layer in any order (CAA, ACA, and AAC) are referred to as Set 2A (shown in the black box of Figure 2.1b). The samples with two **Chr** layers and one **Alk** layer in any order (ACC, CAC, and CCA) are designated Set 2C (in the dark gray box). The samples with an **Alk** layer closest to the channel (CAA, ACA, and CCA) are shown by the dashed green boxes and are named Set A Channel. The samples with a **Chr** layer closest to the channel (ACC, CAC, CCA) are indicated by the dotted purple lines and referred to as Set C Channel. Note that there is still a ZrO_x capping layer between the organic layers and the channel.

2.3.2 SAND Film Morphology

AFM was used to evaluate the surface roughness, contiguity, and quality of all SAND structures. Contact angle studies were used to confirm the self-assembly of the **Alk** molecule. The water contact angle for the ZrO_x primer layer and the **Alk** coated ZrO_x layer is ~20° and ~87°, respectively (Table 2.1). Before the fabrication and assessment of the Zr-SAND-3 structures, AFM was used to investigate the self-assembly of the **Alk** molecule onto the ZrO_x primer layer. The rms roughness of the uncapped **Alk** layer is 0.35 nm (Figure 2.2 and Table 2.2). The ZrO_x capped **Alk** bilayer is smoother with a rms roughness of 0.14 nm (Figure 2.3), which is similar to previous **Chr** based one-layer Zr-SAND (0.15 nm).[15] To ensure that the **Alk** organic layer did not negatively affect further layer growth, a two layer structure with one **Alk** layer and one **Chr** layer was made and demonstrated a rms roughness of 0.18 nm (Figure 2.3 and Table 2.2). To ensure that the **Alk** layer would self-assemble successfully onto a capping ZrO_x layer as well as the primer layer, a two-layer Zr-SAND structure, where both organic layers were **Alk** layers, was grown and had a rms roughness of 0.20 nm (Figure 2.3 and Table 2.2).

Table 2.1. Aqueous Contact Angle vs. Time of Immersion for ZrO_x Coated Si Substrates in **Alk** Solution

Minutes of Self-Assembly	Contact Angle of Water
0	20°
30	85°
60	87°

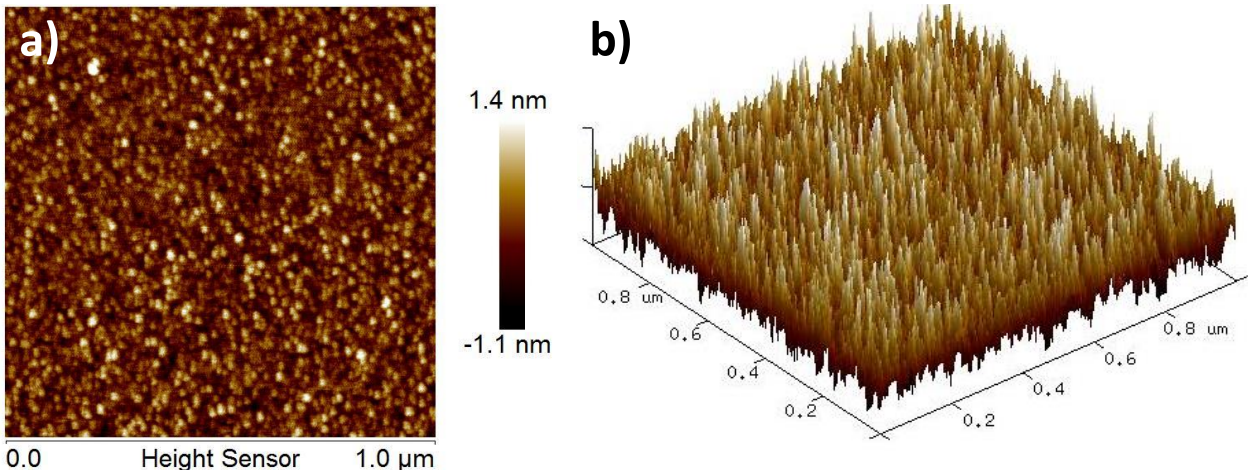

Figure 2.2. AFM Images of Alk Self-Assembled Monlayer. a) AFM images of an uncapped **Alk** self-assembled layer on ~2 nm ZrO_x (rms = 0.35 nm) and b) corresponding 3D image.

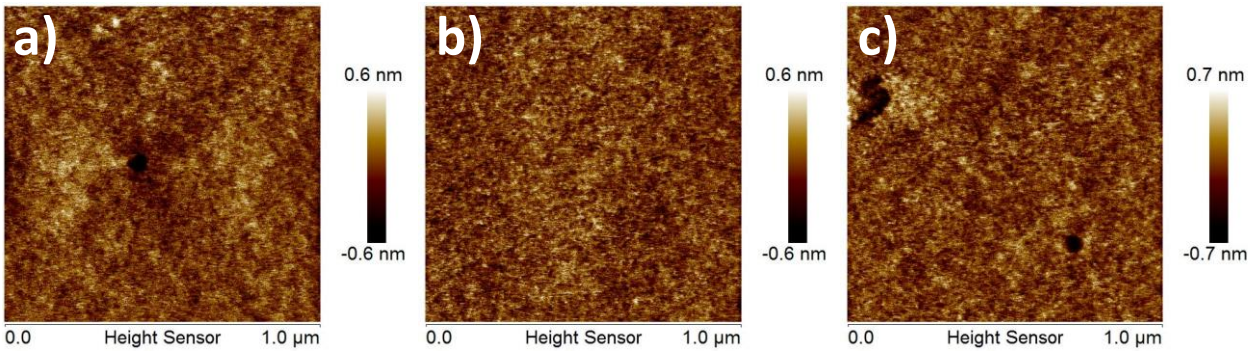

Figure 2.3. AFM Images of Capped One and Two-Layer Zr-SAND. a) AFM of one ZrO_x capped **Alk** layer. RMS = 0.14 nm. b) AFM of AC sample. RMS = 0.18 nm. c) AFM of AA sample with an RMS = 0.20 nm.

Table 2.2. RMS Roughness of the Indicated Dielectric Samples

Sample	Roughness (nm)
Uncapped Alk	0.35
A	0.14
AC	0.18
AA	0.20
CAA	0.132
ACA	0.147
AAC	0.132
ACC	0.135
CAC	0.139
CCA	0.138
2A Average	0.137
2C Average	0.137
A Channel Average	0.139
C Channel Average	0.135

As shown in Figure 2.4, the Zr-SAND-3 structures are smooth, and the average rms roughnesses are 0.132 nm for structure CAA, 0.147 nm for ACA, 0.132 nm for AAC, 0.135 nm for ACC, 0.139 nm for CAC, and 0.138 nm for CCA (Table 2.2), which are comparable to the

roughness of the Si native oxide. There are no notable differences in the roughnesses of these films regardless of whether they are Set 2A or Set 2C structures (average roughness of 0.137 nm for both). There is a slight difference in the average roughnesses for Set A Channel (0.139 nm) and Set C Channel (0.135 nm). The AFM height images also demonstrate that the dielectric films are continuous and free of cracks. The surface quality also indicates that there is uniform coverage of the organic layers regardless of whether they consist of **Alk** or **Chr**. In fact, the surface roughnesses for the alternating organic three-layer structures are lower than previous reported Zr-SAND-3 (0.36 nm) with all **Chr** organic layers.[15] Excellent dielectric surfaces, as seen in these SAND films, are essential for bottom-gate transistors as roughness in the dielectric/semiconductor interface is known to result in decreased mobility due to increased carrier scattering.[32]

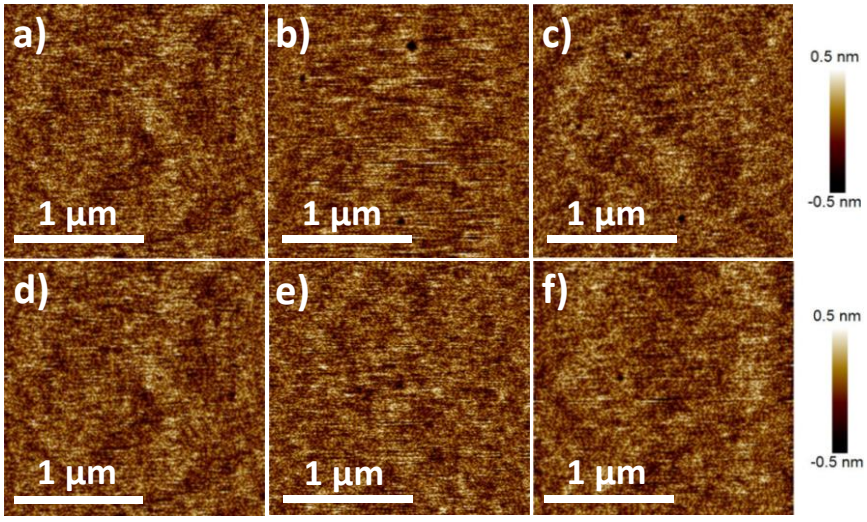

Figure 2.4. AFM Images of Zr-SAND-3 Structures. (a) CAA, (b) ACA, (c) AAC, (d) ACC, (e) CAC, (f) CCA SAND films. All films are smooth with rms roughnesses between 0.13 and 0.15 nm regardless of the differences in the organic layers.

XRR measurements quantify the electron density profile of films in the surface normal direction and are used to assess the thicknesses and quality of the expected layered structures of the various Zr-SAND-3 samples. The initial out of plane reflectivity data ($q = 4\pi\sin\theta/\lambda$) with the best fit model is shown in Figure 2.5. The electron density of the underlying Si substrate (ρ_{Si}) was used to normalize the profiles (Figure 2.6). All of the Zr-SAND samples exhibit the expected oscillations of high- and low-electron density, which correspond to the inorganic and organic components respectively, typical of the hybrid multilayer structures of previous SAND work.[15, 23-24, 27, 33-34] Clearly, the **Alk** self-assembly layers do not disrupt Zr-SAND multilayer film growth. The ZrO_x primer layer thickness is 2.35 ± 0.19 nm, which is consistent with previous Zr-SAND studies (2.1 ± 0.2 nm).[15] The average thickness of the ZrO_x capping layers is 1.28 ± 0.22 nm. However, this average can be further broken down into the thickness of the capping layers within the multilayer and that which forms the final layer of the Zr-SAND structure. The inner and final capping layer *d* values are 1.16 ± 0.17 nm and 1.36 ± 0.10 nm respectively (Table 2.3). This variation reflects the increased annealing and thus densification experienced by the inner capping layers, which has also been previously observed in SAND structures.[24] The Si normalized ZrO_x layer average density is 1.80 which is the same as the bulk crystal values.[24] This indicates that despite the low temperature annealing and solution-processing, the ZrO_x has good densification and is of high quality.

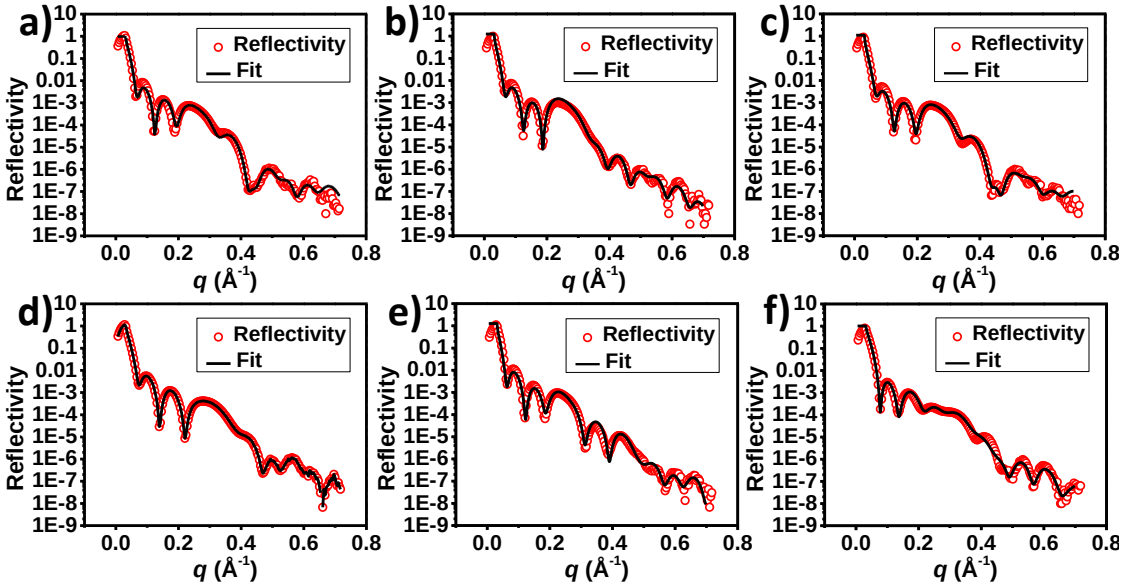

Figure 2.5. XRR Data for Various Zr-SAND-3 Samples. Reflectivity data of a) CAA, b) ACA, c) AAC d) ACC, e) CAC, and f) CCA on Si substrates. The best fit is shown in black.

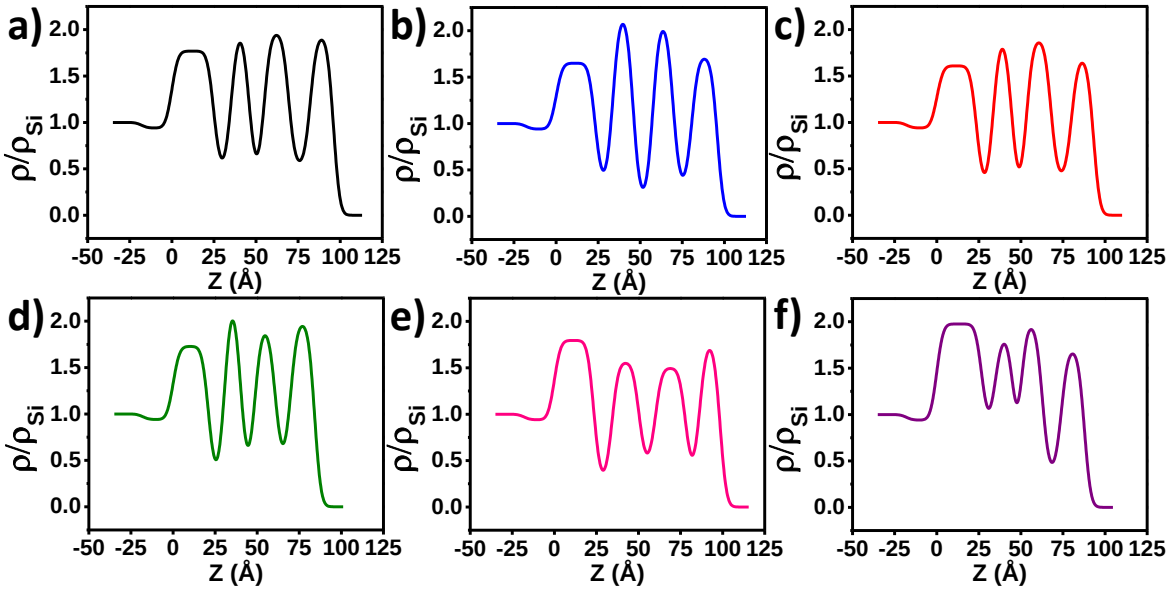

Figure 2.6. Si Normalized Electron Density Profile vs. Height (Z) Above Surface Normal for Various Zr-SAND-3 Samples. The organic and zirconia layers are clearly defined in the XRR scans and are normalized to the underlying Si substrate. (a) CAA, (b) ACA, (c) AAC, (d) ACC, (e) CAC, and (f) CCA.

Table 2.3. XRR Derived Average Layer Thickness

Layer	Thickness Average (nm)
Alk	1.05 ± 0.12
Chr	0.97 ± 0.19
Primer ZrO_x	2.35 ± 0.19
Inner ZrO_x Capping	1.16 ± 0.17
Final ZrO_x Capping	1.36 ± 0.10

The overall thicknesses of Set 2C and Set 2A samples are 9.00 ± 0.75 nm and 9.48 ± 0.16 nm respectively (Table 2.4). Unsurprisingly, given the difference in thickness between Set 2C and Set 2A, the **Chr** layers have an average thickness of 0.97 ± 0.19 nm while that of the **Alk** layers is 1.05 ± 0.12 nm. To further assess the differences between the **Chr** and **Alk** layers, the surface coverages were calculated by dividing the average electron density of the organic layers by the total number of electrons of the corresponding self-assembly component. **Alk** surface coverage was determined to be 2.9 ± 0.5 molecules/nm^2 while the **Ch**r surface coverage was 1.1 ± 0.3 molecules/nm^2. Though the electron densities of the two different organic layers are similar in the XRR (Table 2.6), the difference in the electrons per molecule results in the disparate surface coverages (Table 2.7). The **Chr** molecule has a total electron count that is ~2.8 times greater than the **Alk** molecule, but **Alk** as a 2.6× greater surface coverage than **Chr**, which explains the similarity in the electron densities of the two organic layers.

Table 2.4. Thickness of Zr-SAND-3 Samples Derived from XRR Data

Sample	XRR Derived Thickness (nm)
CAA	9.58
ACA	9.56
AAC	9.30
2A Average	9.48 ± 0.16
ACC	8.39
CAC	9.83
CCA	8.76
2C Average	9.00 ± 0.75

Table 2.5. Sample Thickness Based on Average Layer Thicknesses

Sample	Thickness (nm)
Alk One-Layer Zr-SAND	4.76
Chr One-Layer Zr-SAND	4.66
2A Samples	9.11$^{\perp}$
2A Samples from Overall Averages	9.48 ± 0.16*
2C Samples	9.02$^{\perp}$
2C Samples from Overall Averages	9.00 ± 0.75*

$^{\perp}$Summated from XRR derived thicknesses for each individual layer from Table 2.3

*Average thickness from Zr-SAND-3 XRR data for comparison from Table 2.4

Table 2.6. Average Si-Normalized Electron Density of the Indicated Layers

Layer	Si Normalized Electron Density
ZrO_x	1.80
Alkyl	0.53
Chromo	0.65

Table 2.7. Surface Coverage of Organic Layers

Molecule	Electrons/Molecule	Average Surface Coverage (Molecule/nm^2)
Alkyl	138	2.9 ± 0.5
Chromo	386	1.1 ± 0.3

2.3.3 SAND Dielectric Properties

Metal-insulator-semiconductor (MIS) devices were fabricated to assess the dielectric properties of the various Zr-SAND structures, and all C-V measurements were carried out at 10 kHz. Sol-gel ZrO_x devices were first fabricated on Si substrates by spin-coating two layers of 0.01 M $ZrCl_4$ capping solution and annealing (200 °C for 20 min) after each layer before the deposition of gold contacts. These devices were used to determine the *k* of the ZrO_x. With the reasonable assumption of a native SiO_2 layer thickness of 2.5 nm,[35] the dielectric constant of ZrO_x is 9.4, slightly lower than previously reported (*k* ~10).[35] Note, the ZrO_x film annealing temperature in the previous study was 50 °C lower (150 °C), but the annealing time was 3× longer than that used in the present work (1 hr vs. 20 mins).[35] To assess the viability of the new **Alk** molecule and compare it to **Chr**, one-layer MIS devices were fabricated (Figure 2.7). Modeling the one-layer Zr-SAND devices as capacitors in series,

$$\frac{1}{C_i} = \left(\frac{1}{C_{SiOx}} + \frac{1}{C_{p-ZrOx}}\right) + \left(\frac{1}{C_{Org}} + \frac{1}{C_{c-ZrOx}}\right) \quad \text{(Eq. 4)}$$

where SiO_x is the native oxide on the Si wafer (*k* = 3.9), p-ZrO_x is the primer layer, c-ZrO_x is the capping layer, and Org is the organic layer. The capacitances of the one-layer structures are very similar for **Alk** and **Chr** at 738.7 and 755.5 nF/cm^2, respectively. The **Alk** molecule has a ~2.6 times greater surface coverage than the **Chr** molecule. Because **Alk** and **Chr** are both self-assembled through the same anchoring moiety, phosphonic acid, the increased surface coverage of **Alk** is likely due to its less bulky structure. Using the XRR derived layer thicknesses, the dielectric constant is determined to be 6.2 for the **Alk** layer and 6.8 for the **Chr** layer (Table 2.8).

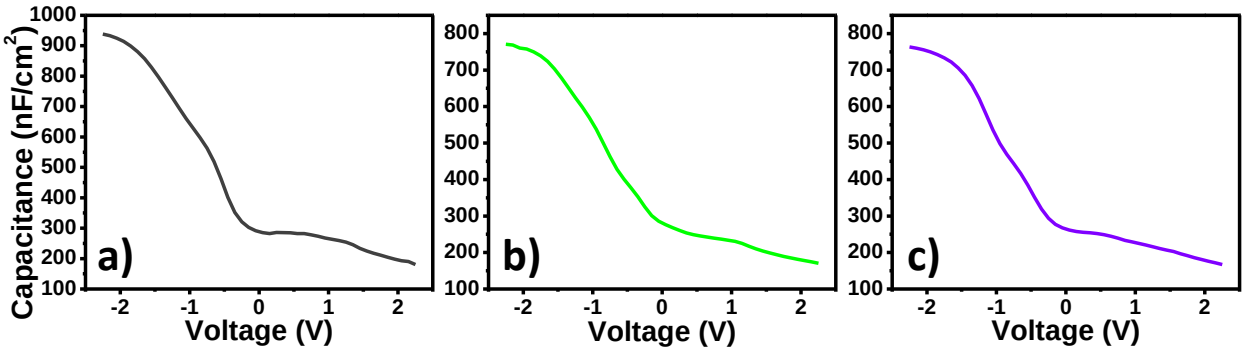

Figure 2.7. Representative Capacitance-Voltage Plots of One-Layer Dielectrics. a) ZrO_x, b) **Alk** one-layer Zr-SAND, and c) **Chr** one-layer Zr-SAND.

Table 2.8. Capacitance and *k* Values for One-Layer Samples

Sample	Capacitance (nF/cm^2)	Thickness of 1 Layer SAND (nm)	Thickness of Sample Layer (nm)	k
ZrO_x	974.6	-	2.35	9.4
Chr	755.5	4.68	0.97	6.8
Alk	738.7	4.76	1.05	6.2

The overall capacitance values of all Zr-SAND-3 devices are exceptionally similar, ranging from 548 to 587 nF/cm^2 (Figure 2.8 and Table 2.9), which is in accordance with previous Zr-SAND work.[15, 26] No trend is observed in the overall capacitance values based on Set 2A and Set 2C, which could reasonably be expected due to the differences in thickness and layer identity (Set 2A = 568 nF/cm^2 and Set 2C = 562 nF/cm^2), or between Set A Channel and Set C Channel. Figure 2.9 (and Table 2.10) shows the average capacitance with the standard deviation for each sample. Each average is taken from at least 35 measurements across multiple batches. The dC/dV values for all samples are very similar (Figure 2.10) indicating that the different number of **Alk** and **Chr** layers, as between Sets 2A and 2C, does not impact the overall capacitance in the accumulation regime. This is unlike the effect seen in Zr-SANDs using organic layers with different inherent

polarizations.[26] Capacitance vs frequency (C-f) measurements were taken from 1 k to 1 M Hz (Figure 2.11). There are no trends between Set 2A and Set 2C or Set A Channel and Set C Channel for the C-f measurements.

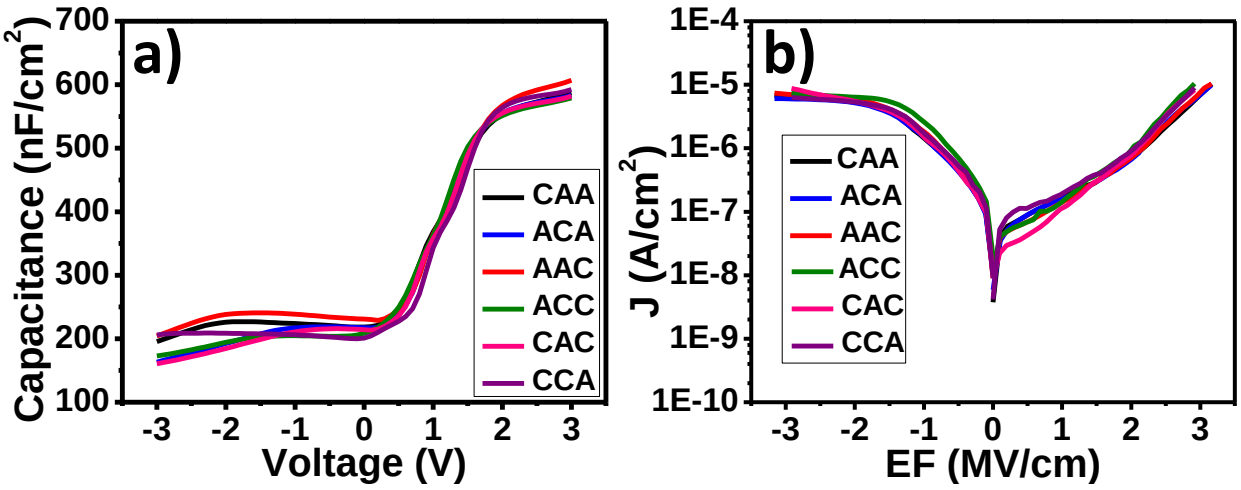

Figure 2.8. Repesentative Capacitance and Leakage Curves for Each Zr-SAND-3 Sample. Importantly, there is essentially no differenation between Set 2A and Set 2C for either the (a) capcitance or (b) leakage plots.

Table 2.9. Physical and Electrical Properties of Zr-SAND Dielectrics with Differing Organic Layer Arrangement

Sample	Thickness (nm)	Roughness (nm)	C_i (nF/cm^2)	J (A/cm^2) at -2 MV/cm	Breakdown (MV/cm)
CAA	9.58	0.132	587	5.70×10^{-6}	-5.66
ACA	9.56	0.147	562	5.18×10^{-6}	-5.13
AAC	9.30	0.132	556	5.82×10^{-6}	-4.60
2A Average	9.48	0.137	568	5.56×10^{-6}	-5.13
ACC	8.39	0.135	584	5.93×10^{-6}	-5.34
CAC	9.83	0.139	554	5.32×10^{-6}	-5.51
CCA	8.76	0.138	548	4.85×10^{-6}	-5.08
2C Average	9.00	0.137	562	5.23×10^{-6}	-5.31

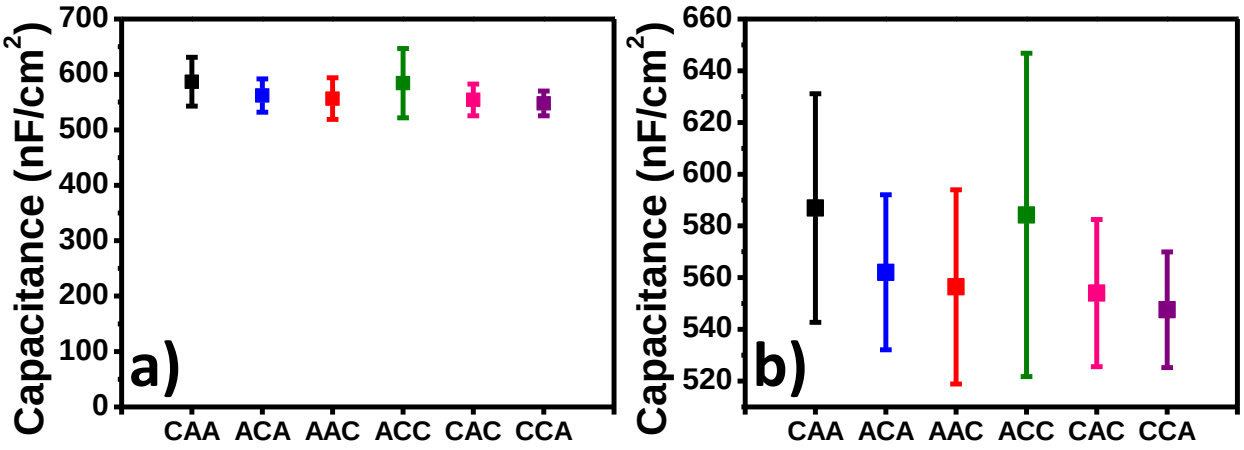

Figure 2.9. Average Capacitance and Standard Deviation for the Indicated Samples.

Table 2.10. Average Capacitance Values for the Indicated Samples

	Capacitance (nF/cm²)	
Sample	**Average**	**St. Dev.**
CAA	586.88	44.21
ACA	562.06	29.96
AAC	556.45	37.54
ACC	584.45	62.53
CAC	554.04	28.47
CCA	547.62	22.35
2A Average	568.46	16.19
2C Average	561.96	19.55

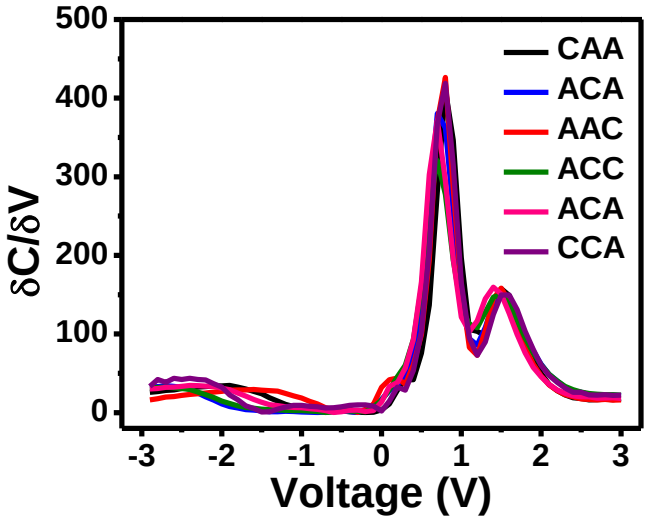

Figure 2.10. Plot of the Derivative of the Capacitance vs. Voltage for Each Zr-SAND-3 Sample.

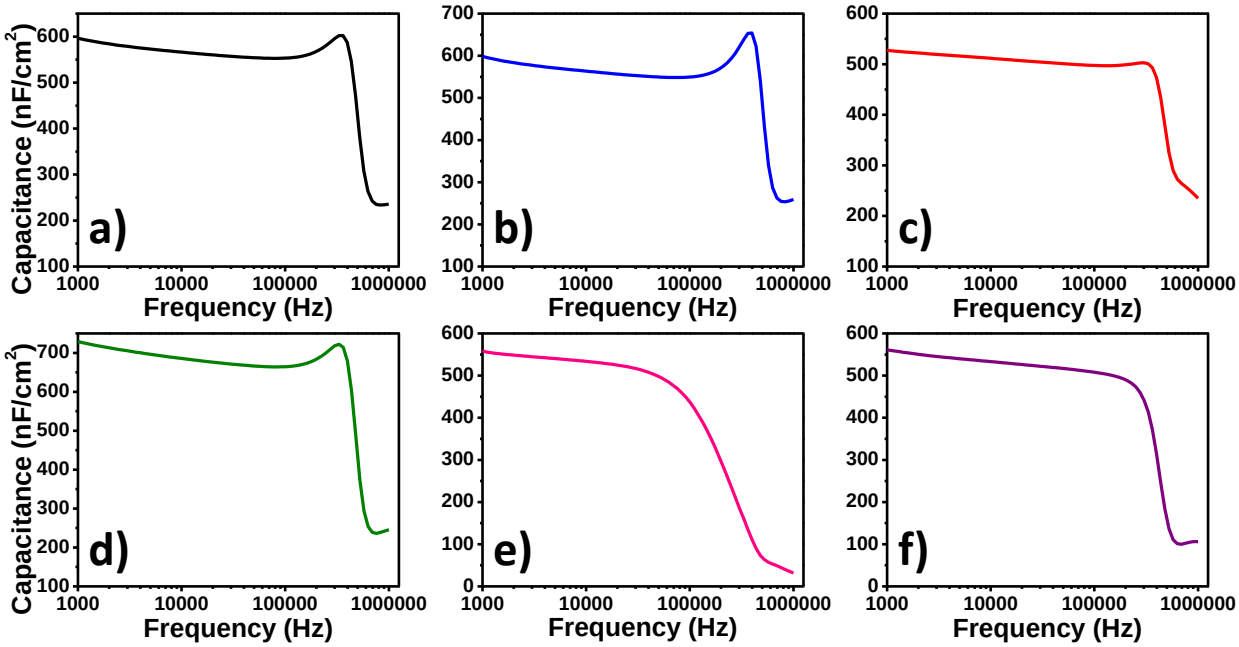

Figure 2.11. Representative Capacitance vs. Frequency Curves for the Indicated Sample. a) CAA, b) ACA, c) AAC, d) ACC, e) CAC, and f) CCA.

The average onset of accumulation in the C-V curves is more positive in Set A Channel than in Set C Channel at 110 mV and 10 mV, respectively (Table 2.11). However, the difference is very small and both averages are well within the standard deviations of the other. This is in contrast to previous Zr-SAND studies where the use of organic layers of oppositely oriented dipoles found significant differences in the onset of accumulation.[26] The interfacial trap densities of the various Zr-SAND-3 samples were calculated from the C-V and conductance-voltage (G-V) measurements.[23, 36-37] Set C Channel has a higher average interfacial trap density (9.68×10^{12} eV^{-1} cm^{-2}) than Set A Channel (8.32×10^{12} eV^{-1} cm^{-2}) as shown in Table 2.12.

Table 2.11. Average Onset Voltage of the Capacitance in Accumulation for the Indicated Samples

	Onset Voltage (V)	
Sample	**Average**	**St. Dev.**
CAA	0.15	0.12
CCA	0.11	0.21
ACA	0.08	0.14
CAC	0.02	0.21
AAC	0.01	0.19
ACC	0.00	0.23
A Channel Average	0.11	0.16
C Channel Average	0.01	0.21

Table 2.12. Average Trap Density for the Indicated Dielectric Samples

	Trap Density (eV^{-1} cm^{-2})	
Sample	**Average**	**St. Dev.**
ACC	1.00E+13	4.62E+12
AAC	9.83E+12	5.34E+12
CAC	9.17E+12	6.22E+12
CAA	8.81E+12	3.64E+12
ACA	8.59E+12	3.94E+12
CCA	7.56E+12	3.36E+12
A Channel Average	8.32E+12	6.68E+11
C Channel Average	9.68E+12	4.47E+11

The MIS structures used for the capacitance measurements were also used for leakage measurements. The Au contact pads are large (200 μm × 200 μm) and thus allow for an accurate assessment of the overall quality of the Zr-SAND-3 films. It is also important to note that the samples were not prepared in a clean room. The average leakage currents at -2 MV/cm are $5.53(\pm2.11)\times10^{-6}$ and $5.36(\pm2.02)\times10^{-6}$ A/cm^2 for Set 2A and Set 2C, respectively (Table 2.9 and Table 2.13). At 2 MV/cm the average leakage current for Set 2A is $6.96(\pm2.96)\times10^{-7}$ and $5.90(\pm2.56)\times10^{-7}$ A/cm^2 for Set 2C (Table 2.13). These leakage values are slightly higher than those previously reported for three-layer Zr-SAND where all of the organic layers consisted of **Chr** (3×10^{-7} A/cm^2).[15] Regardless, the low leakage currents presented in this work indicate that the Zr-SAND-3 structures are still of excellent quality and nearly pinhole free. The high quality of the films is at least partially attributed to the advantages of the iterative nature of the SAND growth process, where defects present in one layer are minimized by the successive layers. As seen in Table 2.14, the leakages in the negative voltage range are similar between Set 2A and Set 2C. However, in the positive voltage range Set 2C has consistently lower leakage currents than Set 2A.

This differentiation is further seen in the dielectric breakdown of the samples (Figure 2.12 and Table 2.15). As shown in Table 2.15, the average breakdowns in negative electric fields are similar for Set 2A (-5.13 MV/cm) and Set 2C (-5.31 MV/cm). Conversely there is significant difference in the average breakdowns in positive electric fields, which are 7.60 MV/cm for Set 2C and 5.82 MV/cm for Set 2A. Given the differences between Set 2A and Set 2C in both the average leakage current and breakdowns, it is obvious that **Chr**'s built-in dipole, which is in opposite alignment with the applied electric field, has a significant impact in reducing the effects of the positive electric fields. This indicates that the inherent dipole of the organic layers within the SAND structure can be tailored to increase the durability to the applied electric fields depending on the operating conditions required. The two samples with the highest breakdown strength, ACC and CCA, both have two adjacent **Chr** layers, suggesting that there is coupling between the highly polarizable organic layers.

Table 2.13. Dielectric Leakage Data at Various Electric Fields for the Indicated Samples

EF (MV/cm)	CAA	ACA	AAC	ACC	CAC	CCA	2A Average	2C Average
-2	5.70E-06	5.18E-06	5.82E-06	5.93E-06	5.32E-06	4.85E-06	5.53E-06	5.36E-06
-3	6.67E-06	6.02E-06	7.05E-06	6.75E-06	8.76E-06	5.88E-06	6.54E-06	7.25E-06
2	7.07E-07	6.73E-07	7.12E-07	4.85E-07	6.97E-07	5.69E-07	6.96E-07	5.90E-07
3	8.00E-06	7.87E-06	6.70E-06	2.99E-06	8.25E-06	3.43E-06	7.53E-06	5.08E-06

Table 2.14. Dielectric Leakage Data at Various Voltages for the Indicated Samples

Voltage (V)	CAA	ACA	AAC	ACC	CAC	CCA	2A Average	2C Average
-1	1.62E-06	1.69E-06	2.01E-06	2.46E-06	1.40E-06	1.63E-06	1.77E-06	1.83E-06
-2	5.86E-06	5.39E-06	5.99E-06	6.33E-06	5.32E-06	5.28E-06	5.75E-06	5.64E-06
-3	6.80E-06	6.06E-06	7.36E-06	7.4E-06	8.76E-06	6.29E-06	6.74E-06	7.48E-06
1	1.78E-07	1.69E-07	1.51E-07	1.36E-07	1.10E-07	1.85E-07	1.66E-07	1.44E-07
2	8.65E-07	8.43E-07	8.79E-07	7.83E-07	6.97E-07	8.05E-07	8.62E-07	7.62E-07
3	1.03E-05	9.91E-06	1.04E-05	1.04E-05	8.25E-06	8.92E-06	1.02E-5	9.19E-06

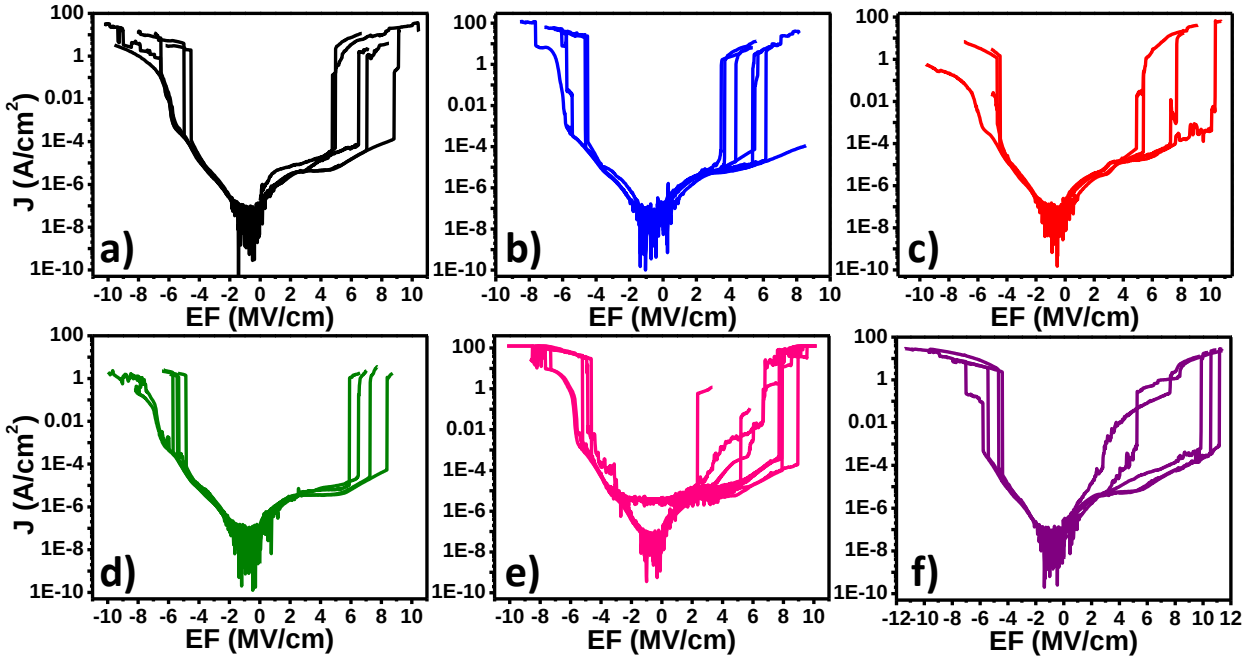

Figure 2.12. Leakage vs. Electric Field Plots Showing Dielectric Breakdown for the Indicated Samples. a) CAA, b) ACA, c) AAC, d) ACC, e) CAC, and f) CCA.

Table 2.15. Dielectric Breakdown Data in EF for the Indicated Samples

Sample	Negative Breakdown (MV/cm)		Positive Breakdown (MV/cm)	
	Average	St. Dev.	Average	St. Dev.
CAA	-5.66	1.04	6.42	1.66
ACA	-5.13	0.68	4.76	1.08
AAC	-4.60	0.14	6.29	1.34
ACC	-5.34	0.36	7.02	1.07
CAC	-5.51	1.22	6.85	2.29
CCA	-5.08	0.65	8.92	2.34
2A Average	-5.13	0.53	5.82	0.92
2C Average	-5.31	0.22	7.60	1.15

2.3.4 Pentacene TFT Characterization

To further understand the effects of the arrangement of the **Alk** and **Chr** organic layers, bottom-gate top-contact OTFTs were fabricated using pentacene as the semiconductor. The ZrO_x surfaces of the SAND samples were left unmodified so that the organic layers within the dielectrics would have the most effect. Pentacene TFTs were also fabricated on ZrO_x primer coated 300 nm SiO_2 to serve as control devices and on OTS coated 300 nm SiO_2 to show that the pentacene purity and deposition parameters produce properly functioning devices (0.31 $cm^2\ V^{-1}\ s^{-1}$). Major TFT device performance metrics are summarized in Tables 2.16. All of the Zr-SAND TFTs exhibit higher mobilities than the OTS-SiO_2 devices despite the fact that the pentacene is deposited directly onto an unmodified metal oxide surface, which is known to increase charge trapping at the dielectric/semiconductor interface for organic semiconductors.[1, 3, 38] The mobilities of the Zr-SAND-3 devices (0.40 – 0.66 $cm^2\ V^{-1}\ s^{-1}$) are also higher than those of the ZrO_x-SiO_2 ones (0.34 $cm^2\ V^{-1}\ s^{-1}$). However, there are no trends in the mobilities corresponding to any grouping of the dielectrics. The mobilities for the Zr-SAND-3 devices in this work are slightly higher than

previously reported pentacene devices on three-layer Zr-SAND with all **Chr** organic layers (0.36 $cm^2\ V^{-1}\ s^{-1}$) and similar capacitance (560 nF/cm^2).[15] The subthreshold slopes (SS), which is a reflection of how quickly a device turns on,[3] of the Zr-SAND TFTs are an order of magnitude lower (180 to 220 mV/dec) than the ZrO_x-SiO_2 control (5740 mV/dec) devices. The interfacial trap densities (D_{it}) at the semiconductor/dielectric interface for the SAND based TFTs (4.37×10^{12} to $7.14 \times 10^{12}\ eV^{-1}\ cm^{-2}$) are comparable to the ZrO_x-SiO_2 control ($5.39 \times 10^{12}\ eV^{-1}\ cm^{-2}$). No trends based on any grouping of the Zr-SAND-3 dielectric samples are seen for the mobility, the SS, or the D_{it}.

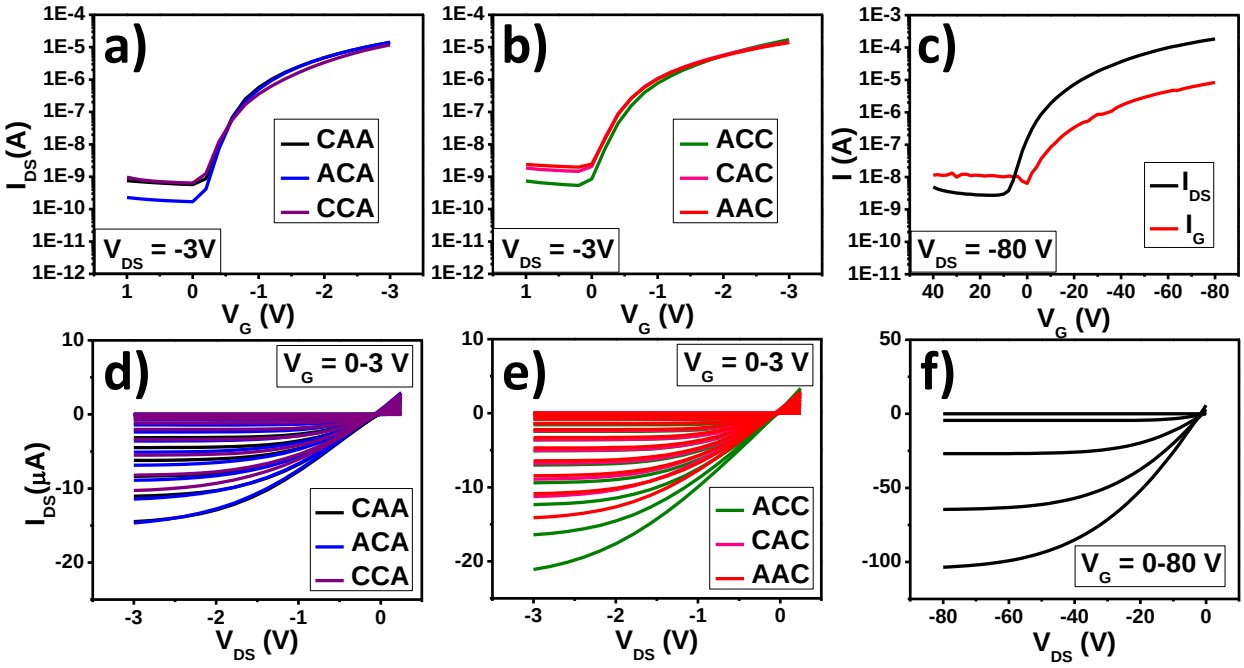

Figure 2.13. Representative Transfer and Output Plots of Pentacene TFTs for the Indicated Samples. Plots are arranged by Sets A Channel (transfer a and output d) and C Channel (transfer b and output e). Pentacene TFTs with a ZrO_x coated 300 nm SiO_2 dielectric transfer (c) and output (f) curves for comparison.

Table 2.16. Electrical Properties of Pentacene TFTs Fabricated on Zr-SAND Dielectrics with Differing Organic Layer Arrangement

Sample	μ ($cm^2 V^{-1} s^{-1}$)	V_{on} (V)	V_{th} (V)	On/Off Ratio	SS (mV/dec)	D_{it} ($eV^{-1} cm^{-2}$)
ACA	0.66±0.14	-0.19±0.06	-0.69±0.06	2.30×10^4	193±55	5.83×10^{12}
CAA	0.51±0.22	-0.14±0.07	-0.59±0.09	2.70×10^4	214±43	6.88×10^{12}
CCA	0.53±0.06	-0.13±0.06	-0.56±0.15	2.69×10^4	182±42	4.37×10^{12}
CAC	0.40±0.08	-0.068±0.09	-0.45±0.11	1.56×10^4	216±48	7.14×10^{12}
AAC	0.49±0.11	-0.078±0.13	-0.45±0.23	1.14×10^4	215±55	5.24×10^{12}
ACC	0.66±0.09	0.055±0.23	-0.43±0.16	1.13×10^4	210±88	6.59×10^{12}
SiO_2-ZrO_2	0.34±0.08	8.77±3.42	5.54±19.33	3.66×10^4	5740±1620	5.39×10^{12}
OTS-300 nm SiO_2	0.31±0.03	-15.7±2.1	-4.73±1.98	1.92×10^6	2018±141	2.40×10^{12}

The V_{th} for the Zr-SAND devices is significantly lower than that of the ZrO_x-SiO_2 control ones, ranging from -0.43 to -0.69 V and 5.54 V, respectively. A V_{th} close to 0 V is suitable for portable devices as less energy is required to turn a device into the on state.[3, 27] It is also important to note that the ZrO_x-SiO_2 control devices display significant variation in V_{th} with a standard deviation of 19.33 V while the highest standard deviation among the Zr-SAND-3 devices is 0.23 V. When comparing the V_{th} within the Zr-SAND-3 structures, a trend emerges (Table 2.17). Set A Channel has a more negative V_{th} compared to Set C Channel, meaning that Set A Channel requires a larger applied voltage to turn on. The same trend is seen in the V_{on} data (Tables 2.16 and 2.17), where the values for Set A Channel are again more negative. However, the actual ordering of the devices from least negative to most negative for V_{th} and V_{on} are different (Table 2.17). The ordering among Set A Channel is unaffected when comparing V_{th} and V_{on} (sample ACA is the most negative for both) unlike Set C Channel. The least negative sample for V_{th} is

AAC while it is ACC for V_{on}. As the application of the concept of V_{th} to organic TFTs is debatable,[3] the V_{on} data is likely more reliable in assessing the devices. This indicates that the arrangement of two **Chr** layers closest to the channel, as in sample ACC, has a cumulative effect on the charges in the channel, but the separation of two **Chr** layers by an **Alk** layer, like in CAC, mitigates this. The diminished effect of the **Chr** layer with distance from the channel is further demonstrated by the V_{on} values within Set A Channel as the presence of one or two **Chr** layers does not present a clear trend (Table 2.17). The V_{on} can often be affected by the D_{it}, as the trap states must first be filled for the device to have sufficient current to enter the on-state. Given that there is no corresponding trend in the D_{it}, it is not the source of the trend seen for the V_{on}. This indicates that having a **Chr** organic layer closest to the semiconductor/dielectric interface, as in Set C Channel, induces more mobile charges. The larger I_{DS} currents measured in Set C Channel sweeping the V_{DS} from 0.5 to -3 V at a gate voltage of 0 V, of which ACC has the highest, further confirms this data (Figure 2.14). Higher dielectric capacitances are known to induce increased charge carriers in the channel,[3] but given the remarkably similar capacitances of all of the Zr-SAND-3 structures, this can be eliminated as a possible cause for the observed V_{on} differences. Previous studies have used SAMs molecules of various dipoles to change the carrier densities in the channel.[39-40] V_{th} shifts achieved through the dipole effects of SAMs, and the corresponding built in electric fields, which modify to the externally applied gate voltage, are widely known.[40-42]

Table 2.17. Pentacene TFT Data That Show Trends Based on Set A Channel and Set C Channel Groupings

Sample	V_{th} (V)	Sample	V_{on} (V)	Sample	On/Off Ratio
ACA	-0.69±0.06	**ACA**	-0.19±0.06	**CAA**	2.70×10^4
CAA	-0.59±0.09	**CAA**	-0.14±0.07	**CCA**	2.69×10^4
CCA	-0.56±0.15	**CCA**	-0.13±0.06	**ACA**	2.30×10^4
CAC	-0.45±0.11	**AAC**	-0.078±0.13	**CAC**	1.56×10^4
ACC	-0.45±0.23	**CAC**	-0.068±0.09	**AAC**	1.14×10^4
AAC	-0.43±0.16	**ACC**	0.055±0.23	**ACC**	1.13×10^4
ZrO_x-300 nm SiO_2	5.54±19.33	**ZrO_x-300 nm SiO_2**	8.77±3.42	**ZrO_x-300 nm SiO_2**	3.66×10^4
A Channel Average	-0.61±0.07	**A Channel Average**	-0.15±0.03	**A Channel Average**	2.56×10^4
C Channel Average	-0.44±0.01	**C Channel Average**	-0.03±0.07	**C Channel Average**	1.27×10^4

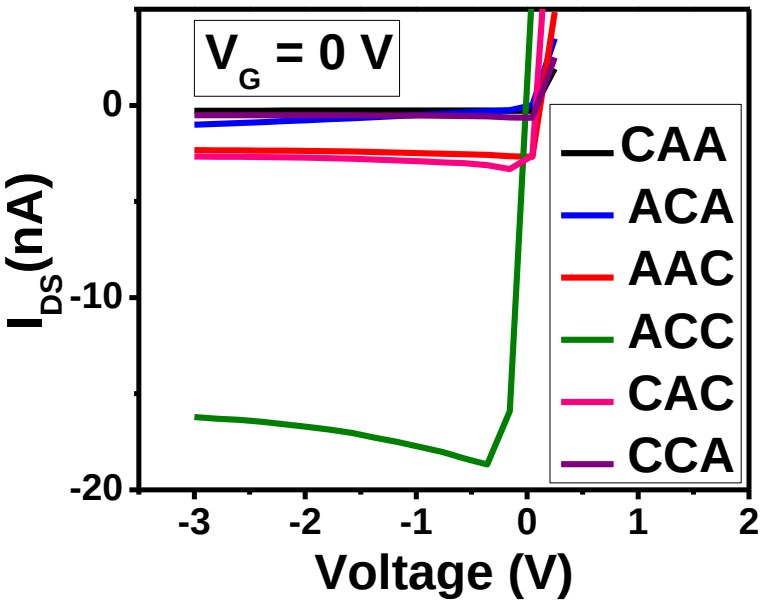

Figure 2.14. Source-Drain Current vs. Drain Voltage for Pentacene Transistors at Zero Gate Voltage on Each Zr-SAND-3 Structure. Higher currents are seen for Set C Channel indicating that larger amounts of carriers are induced in the channel.

The current on/off ratio, which is the difference between the on current and off current in a device, also shows variation between Set A Channel and Set C Channel. Set A Channel has an average on/off ratio of 2.56×10^4 while Set C Ending has an average of 1.27×10^4 (Table 2.16). The ZrO_x coated 300 nm SiO_2 TFTs exhibit the highest on/off ratio, with an average of 3.66×10^4, due to the larger drain field (~ 27x) than those of the SAND-based devices. Note, all devices have the same channel dimensions. However, it should be noted that despite a difference in thickness of ~290 nm, the gate leakage for the ZrO_x-SiO_2 control devices is higher than those for the SAND based TFTs when compared at the extremes of the bias window (-3V for SAND and -80 V for ZrO_x-SiO_2) and at -2 MV/cm as seen in Table 2.18. There is no trend in the on current for the Zr-SAND TFTs which range from 1.15×10^{-5} to 1.72×10^{-5} A (Table 2.19). Since the on currents are very similar and do not follow the same trends as the on/off ratios, the observed grouping is attributed to the off current. Again, this relates to the greater amount of charges induced in the channel in Set C Channel as opposed to Set A Channel (Figure 2.14).[39-40]

Table 2.18. Gate Leakage Current for TFTs Based on the Indicated Dielectrics

Sample	I_{Gate} (A) at -3 V	Sample	I_{Gate} (A) at -2 MV/cm
AAC	4.15×10^{-7}	**ACC**	1.37×10^{-7}
CAC	5.66×10^{-7}	**CCA**	1.64×10^{-7}
CAA	5.78×10^{-7}	**AAC**	1.83×10^{-7}
CCA	6.04×10^{-7}	**ACA**	2.45×10^{-7}
ACC	6.58×10^{-7}	**CAA**	2.53×10^{-7}
ACA	6.63×10^{-7}	**CAC**	2.60×10^{-7}
ZrO_x-300 nm SiO_2	$8.35\times10^{-6*}$	**ZrO_x-300 nm SiO_2**	4.17×10^{-6}
OTS-300 nm SiO_2	$5.06\times10^{-7*}$	**OTS-300 nm SiO_2**	3.24×10^{-7}

*at -80 V

Table 2.19. On Current for OTFTs Fabricated on the Indicated Dielectrics

	On Current (A) at -3 V	
Sample	**Average**	**St. Dev.**
ACA	1.72×10^{-5}	9.39×10^{-7}
ACC	1.52×10^{-5}	2.56×10^{-6}
AAC	1.38×10^{-5}	1.22×10^{-6}
CAC	1.28×10^{-5}	1.50×10^{-6}
CAA	1.21×10^{-5}	1.72×10^{-6}
CCA	1.15×10^{-5}	9.69×10^{-7}
ZrO_x-300 nm SiO_2	$2.19\times10^{-4*}$	$2.38\times10^{-5*}$
OTS-300 nm SiO_2	$1.64\times10^{-4*}$	$8.26\times10^{-6*}$

*at -80 V

Finally, to ensure that the observed differences in the Zr-SAND based TFTs are not due to differences in semiconductor morphology, AFM was used to image the pentacene films deposited on the different gate dielectrics (Figure 2.15). Since the dielectric surface roughness greatly impacts the charge transport in pentacene transistors,[18, 32, 43] the smooth surfaces of the bare Zr-SAND-3 dielectrics (0.132 to 0.147 nm rms roughness) do not contribute to the differences observed in the TFT metrics (Figure 2.4). The pentacene films on the Zr-SAND and ZrO_x-SiO_2 (Figures 2.15 and 2.16) samples show the dendritic growth typical on hydrophilic and high energy surfaces such as ZrO_x.[18, 44-46] No significant differences in the crystallites on the Zr-SAND samples are observed. The morphology of the pentacene on OTS coated SiO_2 shows a different growth mode characteristic of pentacene deposited on hydrophobic and low energy surfaces, but still demonstrates that the pentacene deposition conditions produced functioning transistors (Figure 2.16).[18, 44-46] The similarities in the AFM performed on the bare Zr-SAND dielectrics and on the

deposited pentacene films eliminate morphological differences as the source of the trends observed in the TFT metrics.

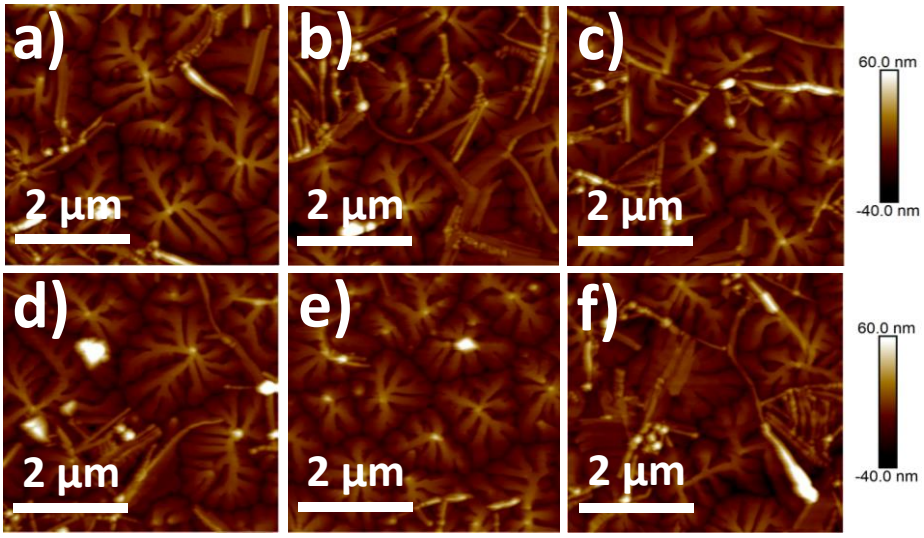

Figure 2.15. AFM of Pentacene Films for the Indicated Samples. a) CAA, b) ACA, c) CCA, d) ACC, e) CAC, and f) AAC. Note the dendritic growth of the pentacene crystallites on the ZrO_x topped SAND structures.

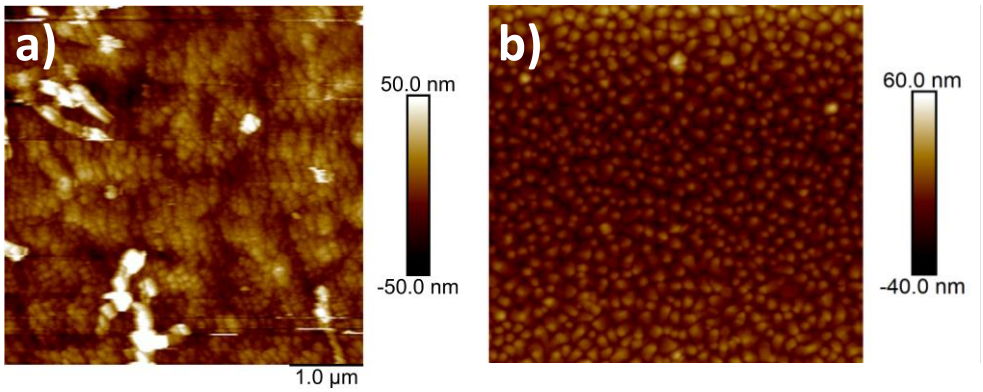

Figure 2.16. AFM of Pentacene Films on ZrO_x Coated 300 nm SiO_2 and OTS Coated 300 nm SiO_2. The differences between the dendritic growth of the pentacene crystallites on the ZrO_x coated sample (a) and the smaller crystallite growth on the OTS (b) are clear. The film in (a) is of lower quality because it was taken after contact deposition and TFT testing.

2.4 Conclusions

This study demonstrates that the complex interactions between the organic layers within the SAND structure contribute to many of the unconventional hybrid dielectric's unique characteristics. By using a self-assembly molecule based on an alkyl chain (**Alk**) and one derived from a stilbazolium core (**Chr**) in alternating layered structures, the effects of the built-in dipole moment of the highly polarizable **Chr** on the nature of the capacitors and TFTs are observed. The various Zr-SAND dielectric structures were characterized by AFM and XRR, which demonstrates smooth surfaces ideal for bottom-gate devices and the regular layered structure, respectively. The capacitance and leakage measurements showed that the built-in dipole moment of the **Chr** layer has a significant impact on the breakdown strength in the positive voltage regime where the **Chr** dipole moment is oriented opposite to the field. Additionally, there is evidence of coupling between adjacent **Chr** layers producing even greater breakdown strength. The pentacene TFT

devices showed Set A Channel had a more negative V_{on}, requiring a higher voltage to turn on compared to Set C Channel. A decreased on/off ratio of the devices in Set C Channel was also observed. Both trends are indicative of increased carrier generation in Set C Channel TFTs, regardless of the similar capacitances for all of the Zr-SAND films. For both the V_{on} and the on/off ratio, interactions between two adjacent **Chr** layers enlarged these effects. This work provides a deeper understanding of the complex effects and interactions of the organic layers within the SAND structure and thus the tailorability of this already versatile dielectric family.

Chapter 3

Self-Assembled Nanodielectrics for Solution-Processed Top-Gate Amorphous IGZO Thin-Film Transistors

3.1 Background

Solution-processing of functional electronic materials for optoelectronic devices is a viable emerging strategy for technologies that require large-area coverage, low manufacturing cost, and/or mechanical flexibility.[1−3] Representative applications include display backplanes, radio-frequency identification tags, smart windows, and high-volume sensor arrays.[3] To this end, several diverse electronically active and passive material systems are emerging, including organics, metal oxides, nanomaterials, and organic−inorganic hybrids. Achieving the optimum combination of semiconductors, dielectrics, contacts, interconnects, encapsulation/passivation, and substrates with the most suitable architectures for a given application is currently one of the key challenges in this rapidly developing field.[4−6]

Two promising solution-phase approaches recently developed for the low-temperature growth of high-performance dielectric and semiconductor films are the self-assembly of organic−inorganic hybrid nanodielectrics (SANDs)[7,8] and the combustion synthesis of metal oxides.[9,10] SANDs feature nanolayers of inorganic oxide dielectrics such as SiO_x, ZrO_x, and HfO_x, interleaved with highly polarizable conjugated organic molecules, e.g., phosphonic acid derivatives of stilbazolium salts, which undergo self-assembly onto the inorganic nanolayers. This platform of durable materials provides high gate capacitances in TFT devices, lower gate leakage currents than the neat solution-processed inorganic films, chemical and thermal stability, suppression of trapped charge, radiation hardness, and dielectric thicknesses ideal for device scaling.[7,8,11] Combustion synthesis of metal oxide films has been shown to lower the processing temperature requirements for the growth of diverse semiconducting oxides, including In_2O_3, In-Zn-O, and In-Ga-Zn-O (IGZO).[9,12] This is achieved by including an oxidizer (e.g., NO_3^-) and a

fuel (acetylacetone) in the metal oxide precursor solution, which promotes a highly exothermic film growth reaction, thereby achieving efficient oxide network condensation and carbon impurity removal.[9]

The broad compatibility of SANDs with diverse semiconductors has been demonstrated with pentacene,[7] printed IGZO,[13] graphene,[11] and carbon nanotubes.[14] These pairings have yielded impressive TFT mobilities and other important device metrics. Furthermore, the advantages are not only the broad array of compatible unconventional semiconductors but the tailorability of the SAND structure itself in regard to both the inorganic[6–8] and organic components as well.[15,16] Note that IGZO is currently the most important manufactured metal oxide semiconductor material, and sputtered IGZO TFTs have been implemented in many commercial devices.[3] In previous studies, we demonstrated combustion synthesis as a route to high-quality amorphous IGZO (a-IGZO) films from precursor solutions.[17,18] Furthermore, we showed that the combination of combustion-processed a-IGZO with HfO_x-based SAND (Hf-SAND) in a bottom-gate top-contact TFT architecture affords impressive device metrics such as $\mu_{SAT} = 20.6 \pm 4.3$ cm^2 V^{-1} s^{-1}, $V_{th} = 0.0$ 76 V, on current to off current ratio (I_{on}:I_{off}) = 10^7, and SS = 125 mV/dec.[13] Interestingly, the question of why a-IGZO/Hf-SAND devices afford superior TFT performance over analogous devices fabricated with a-IGZO and similar thicknesses of ALD HfO_2 (μ_{SAT} = 2 cm^2 V^{-1} s^{-1}) is not currently resolved but indicates that there are additional performance enhancements from Hf-SAND that likely reflect charge-trapping effects moderated by the polar organic layers.[11]

Top-gate TFT devices offer many attractions over bottom-gate architectures, especially for metal oxide semiconductors.[19,20] Oxides are well known to react with atmospheric oxygen and water, and top-gate structures enable the dielectric to passivate the oxide surface by functioning as

an encapsulation layer, thus making device response more uniform.[21–24] Top-gate IGZO TFTs have been reported with several classes of insulators including polymers and metal oxides. Polymer dielectrics offer mechanical flexibility and solution-processing at low temperatures; however, they typically exhibit low dielectric constants (*k*), excessive gas/H_2O permeability, and limited thermal stability.[7,25,26] Inorganic dielectrics offer high *k* values and environmental stability but generally require either capital-intensive vacuum deposition or high annealing temperatures, which can compromise the underlying semiconductor.[7,25,26] While solution-processed SANDs combine many of the attractions of both inorganic and organic dielectrics and minimize many of their limitations,[5,7,8,26] they have never been implemented in top-gate devices due to fabrication challenges.

In this contribution, we demonstrate the first use of solution-processed SANDs in top-gate bottom-contact (TG-BC) oxide TFT structures. We first establish that SANDs can be grown successfully on combustion-processed a-IGZO films while preserving well-defined nanostructures, as verified by optical spectroscopy (UV−Vis), AFM, X-ray reflectivity (XRR), and cross sectional-TEM measurements. In addition, Hf-SAND properties are assessed in metal−insulator−metal device structures via impedance spectroscopy. Finally, top-gate a-IGZO/Hf-SAND TFTs are fabricated and are shown to exhibit impressive device metrics such as a μ_{SAT} = 19.4 ± 0.5 $cm^2\ V^{-1}\ s^{-1}$, V_{th} = 0.83 ± 0.04 V, log(I_{on}:I_{off}) = 4.26 ± 0.31, and SS = 293 ± 22 mV/dec.

3.2 Experimental Section

3.2.1 SAND Film Fabrication

$HfCl_4$ (99.9+%, sublimated, Sigma-Aldrich) was stored under vacuum when not in use to prevent the absorption of water. An initial 0.1 M HfO_x solution was prepared with 93.7 mg of $HfCl_4$ and 4 mL of 100% ethanol. The solution was stirred at room temperature for 5 minutes before the addition of 264 μL of nitric acid. The 0.1 M solution was stirred at 50 °C for 3 hours and then at 25 °C for at least 12 hours. The initial 0.1 M HfO_x solution was then diluted to 0.01 M or 0.02 M HfO_x using absolute ethanol. The diluted solutions were aged while stirring for at least 30 minutes. ITO substrates were sonicated in acetone, hexanes, and absolute ethanol for at least 10 min each before being plasma cleaned for 5 minutes at 400−500 mTorr. SAND growth was carried out in a HEPA-filtered laminar flow clean hood (NuAire), which contained plasma cleaning, spin coating, annealing, and self-assembly apparatus. All HfO_x solutions were passed through a 0.2 μm Teflon syringe filter during the spin-coating process. The 0.02 M HfO_x was spin-coated directly onto the ITO substrates at 5000 rpm for 30 seconds to produce the HfO_x primer layer. The substrates were then annealed at 200 °C for 20 minutes. The 4-[[4-[bis(2-hydroxyethyl)-amino]phenyl]diazenyl]-1-[4-(diethoxyphosphoryl) benzyl]-pyridinium bromide (PAE) used for the organic layers was synthesized in this laboratory as previously described.[7] A 3.0 mM solution of PAE in methanol was used for the organic layer self-assembly. The primer layer coated substrates were submerged in the PAE solution at 60 °C for 1 hour. The substrates were then sonicated in methanol for 5 minutes before being individually sonicated in fresh methanol for 1 minute. The capping layer was next spin-coated with the 0.01 M HfO_x solution on top of the organic layer and annealed in the same manner as the primer layer. These steps were repeated to

achieve four-layer SAND stacks. Additional SAND structures were produced on Si/SiO_x substrates for the AFM and XRR characterization and on glass for UV−Vis measurements. These substrates were prepared with two layers of combustion-processed a-IGZO before the SAND deposition. The a-IGZO preparation is described in section 3.2.4. Transistor Fabrication and Electrical Measurements.

3.2.2 SAND Film Characterization

X-ray reflectivity (XRR) measurements were performed on a 9 kW Rigaku Smartlab Workstation. X-rays were generated from the Cu rotating anode (X-ray wavelength is 1.542 Å) and collimated to produce a monochromated X-ray beam with dimension 0.1 × 5 mm and flux ∼3 × 10^8 cps at the sample surface. The XRR data were modeled and fitted by using the Motofit package[27] to obtain electron density profiles, which contain information on the thickness, electron density, and interfacial roughness of each layer. The UV−Vis spectra of SAND films on ITO substrates were obtained on a Varian Cary 50 Scan spectrophotometer. AFM measurements were made on a Bruker 550 Dimension FastScan AFM. Cross-sectional transmission electron microscopy (CS-TEM) images were collected using a Hitachi HD-2300 Dual EDS Cryo STEM. The CS-TEM samples were prepared directly from actual TFT devices with standard focused ion beam (FIB) milling techniques (FEI Helios NanoLab 600). A ∼2 μm-thick platinum layer was deposited prior to the ion milling to protect samples from ion beam damage.

3.2.3 SAND Film Electrical Measurements

Metal−insulator−metal (MIM) capacitors were fabricated on four-layer Hf-SAND stacks on ITO substrates. Gold contacts (200 μm × 200 μm) were deposited via thermal evaporation

(Denton) through shadow masks. An Agilent B1500A semiconductor parameter analyzer was used for MIM characterization under ambient conditions. A flexible tungsten whisker probe (SE-SM, Signatone) served as the cathode while a beryllium-copper alloy probe (SE-BC, Signatone) served as an anode for the capacitance vs voltage (C−V) curves and the leakage current density vs voltage (J−V) curves. The C−V curves were performed at 10 kHz. The C−f curves (1 to 100 kHz) were measured using an Agilent 568 B1500A, while the curves ranging from 100 Hz to 100 kHz were performed using a Biologic SP-1500.

3.2.4 Transistor Fabrication and Electrical Measurements

Cr/Au (5 nm/30 nm) source/drain contacts were evaporated (Denton) at a base pressure of 3×10^{-6} Torr onto silicon substrates with a 300 nm thermal oxide layer (WRS) and patterned by lift-off using a Suss MABA6 Mask Aligner (L_{ds} = 50 μm, W_{ds} = 150 μm). All solution materials were obtained from Sigma-Aldrich unless otherwise stated. The following metal salts were used: indium(III) nitrate hydrate [$In(NO_3)_3 \cdot xH_2O$], gallium(III) nitrate hydrate [$Ga(NO_3)_3 \cdot xH_2O$], and zinc nitrate hydrate [$Zn(NO_3)_2 \cdot xH_2O$]. All salts were 99.999% pure by trace metal basis and stored under vacuum when not in use. The IGZO precursor solutions were prepared by dissolving metal nitrates in 2-methoxyethanol to produce 0.05 M solutions (10 mL; M = In, Ga, and Zn). The addition of 32 μL of acetylacetone (≥99%) and 30 μL of NH_3 (28% NH_3 in H_2O, ≥99.99 trace metal basis) to each solution was performed immediately. The solutions were aged for ~16 hours before being mixed in the correct atomic ratio (72.5:7.5:20 In:Ga:Zn). The substrates with the patterned contacts were sonicated in ethanol for 10 minutes before being plasma-cleaned for 5 minutes (400−500 mTorr) in preparation for spin-coating. The final IGZO solution was passed through a 0.2 μm Teflon filter as part of the spin-coating process. IGZO was deposited at 3500

rpm for 30 seconds and annealed at 300 °C in air for 20 minutes. Spin-coating and annealing were repeated twelve times to achieve the desired semiconductor thickness. IGZO was then photolithographically patterned and etched with oxalic acid (10% in water) to isolate the devices. The four-layer Hf-SAND was grown as described in section 3.2.1 SAND Film Fabrication. Au gate electrodes (40 nm) were deposited and patterned by lift-off. The completed TFTs were evaluated using an autoprober to test the devices with automatic sorting and parameter extraction. I−V measurements were made with a Keithley 4200. The standard field effect transistor model was used to extract the saturation regime carrier mobilities (μ_{SAT}). Output plots were performed using an Agilent B1500A semiconductor parameter analyzer. All devices were tested in an ambient atmosphere and temperature. The TFT metrics were obtained from the average of eight devices across two batches.

3.3 Results and Discussion

3.3.1 Hf-SAND on a-IGZO Growth

Figure 3.1 shows the fabrication scheme for top-gate bottom-contact a-IGZO/Hf-SAND TFT devices. Briefly, chromium/gold source and drain contacts were evaporated onto SiO_2 substrates by photolithography, where the chromium serves as an adhesion layer for the gold. Combustion-processed a-IGZO was then deposited by spin-coating the precursor solution followed by a brief annealing step (20 minutes) at 300 °C. Oxalic acid was used to etch/pattern the a-IGZO channel. The initial HfO_x priming layer needed for the assembly of the four-layer Hf-SAND film was deposited by spin-coating and then annealed at 200 °C. The HfO_x layers are not combustion-processed like a-IGZO. Previous Hf-SAND work used XPS to compare the O 1s peak

in films processed at both 150 and 300 °C, which were found to be similar and dominated by Hf-O-Hf networks.[6] The XPS measurements also showed that there was no remaining chloride in the film and that despite the low processing temperature, good quality HfO_x layers were formed.[6] The organic stilbazolium constituent, PAE, was self-assembled onto the HfO_x primer layer. The PAE self-assembly was followed by the deposition of a thin HfO_x capping layer. The PAE/capping HfO_x deposition steps were then repeated another three times. Each PAE and capping HfO_x deposition forms an inorganic/organic bilayer. The thin HfO_x layers are not self-assembled onto the PAE layers as the oxide is deposited by spin-coating, not immersion. However, the terminal hydroxyl groups of PAE are expected to react with the capping HfO_x layer subsequently spin-coated onto the organic layer, which doubtlessly contributes to the robust character of the multilayer SAND structures. The deposition of the thicker HfO_x primer layer followed by a total of four bilayers comprises the Hf-SAND-4 gate dielectric employed here. Finally, gold gate electrodes were photolithographically patterned and evaporated to complete the TFT structures.

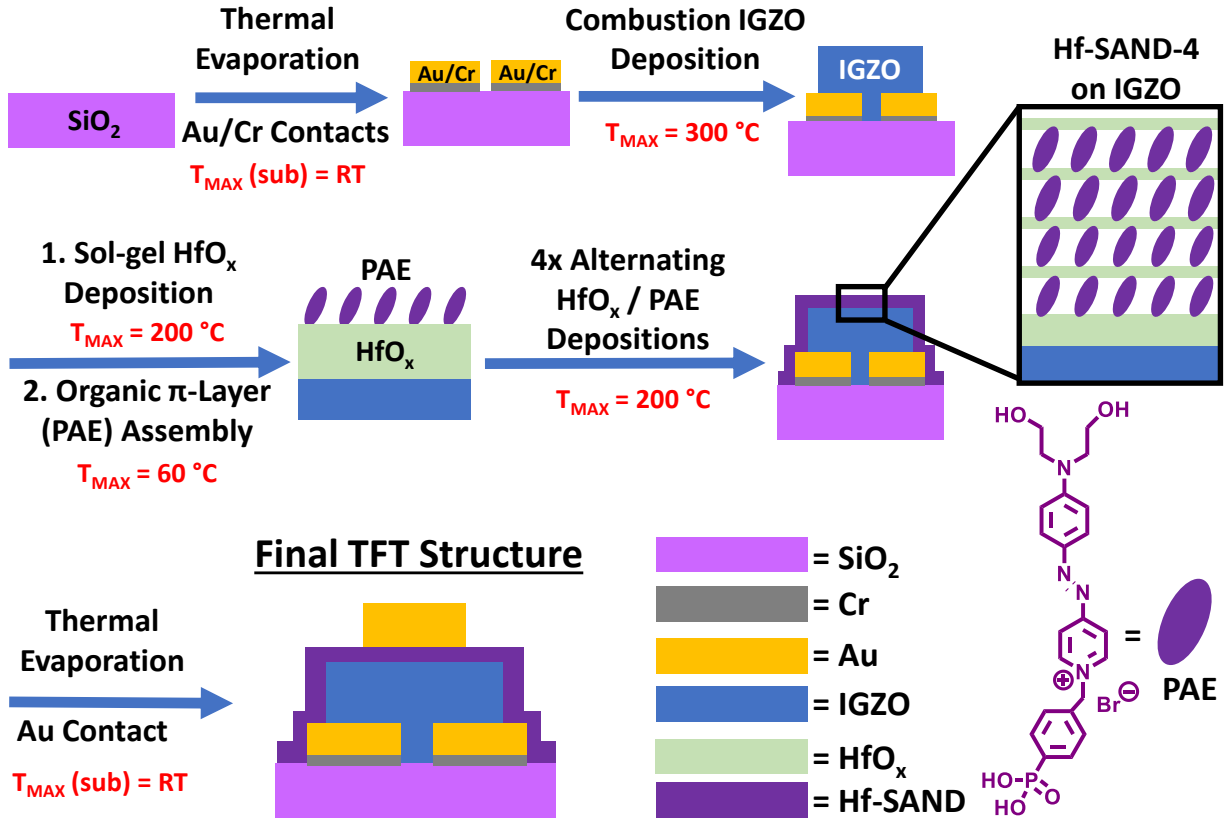

Figure 3.1. Fabrication Scheme for Top-Gate a-IGZO/Hf-SAND-4 TFTs. The maximum processing temperature of each step is indicated. Note that components are not drawn to scale.

3.3.2 Hf-SAND on a-IGZO Characterization

Before TFT device fabrication, the Hf-SAND films were characterized by UV−Vis optical absorption spectroscopy, AFM, X-ray reflectivity (XRR), and cross sectional-TEM (CS-TEM). Although SANDs of different types have been fabricated on glass and doped Si substrates for bottom-gate TFTs,[6,13] it was not obvious that gate insulator quality Hf-SAND films could be grown on a-IGZO. It was expected that PAE would self-assemble directly onto the IGZO surface.[28,29] However, previous work comparing zirconia-based SAND (Zr-SAND) and Hf-SAND indicated that the composition of the metal oxide affects the self-assembly in terms of regular surface

coverage. Hf-SAND had a 30% greater surface coverage compared to Zr-SAND, resulting in an overall higher *k* for the PAE layers.[6] Since good surface coverage of PAE is essential to the further SAND layer growth and electrical performance, a thin HfO_x primer layer was utilized in this work.

Additionally, the fabrication of top-gate structures requires intricate patterning not necessary for the simple common bottom-gate TFTs fabricated previously,[6−8,11,13] further challenging Hf-SAND processing. Thus, a-IGZO-coated glass substrates (~8 nm thick deposited by spin-coating combustion synthesis) were first investigated for sequential Hf-SAND film bilayer growth, and the resulting films were characterized by UV−Vis spectroscopy. The absorption spectra in Figure 3.2 verify the uniform layer-by-layer growth of the SAND multilayer stack on a-IGZO. The absorption increases linearly at 575 nm, where PAE absorption is greatest (Figure 3.2b), indicating that uniformly oriented PAE molecules assemble in effectively equal densities on each sublayer, as is seen in previous analysis of Zr-SAND growth on glass.[7] The Hf-SAND spectra show a slight shift in the PAE peak maxima to lower wavelengths as the number of layers increases, which may reflect slight changes in chromophore aggregation and/or tilt angle.

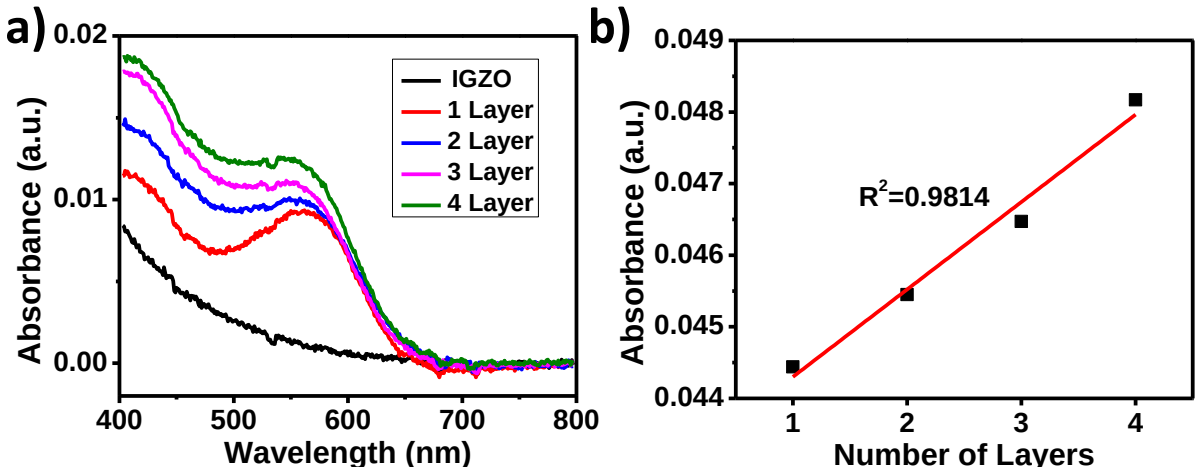

Figure 3.2. UV-Vis Absorption Spectra and Analysis of Absorption at 575 nm for Hf-SAND Films. UV-Vis absorption spectra of Hf-SAND films on a-IGZO/ITO (a). Optical absorption of Hf-SAND films at 575 nm vs. number of layers (b).

Next, AFM images of Hf-SAND on a-IGZO/Si substrates were used to assess the SAND surface topology after each bilayer deposition step. The underlying a-IGZO has a rms roughness of only 0.184 nm (Figure 3.3), which is consistent with previously reported combustion-processed metal oxide films.[9,30–32] As shown in Figure 3.4, the films remain continuous and smooth after each bilayer deposition and, as expected, have slightly greater roughnesses than in bottom-gate structures.[6] The rms roughnesses for the top-gate Hf-SAND samples are 0.329 nm for one bilayer, 0.266 nm for two bilayers, 0.356 nm for three bilayers, and 0.253 nm for four bilayers, while the previously reported roughness values for bottom-gate Hf-SAND multilayers are 0.13−0.17 nm for one to four bilayers.[6] The exceptionally smooth Hf-SAND surfaces assembled on a-IGZO indicate that the films have an overall good quality and that the interfaces between the semiconductor and dielectric layers are likely to be excellent with negligible defects, which is essential to minimize carrier scattering and ensure good TFT metrics.[33]

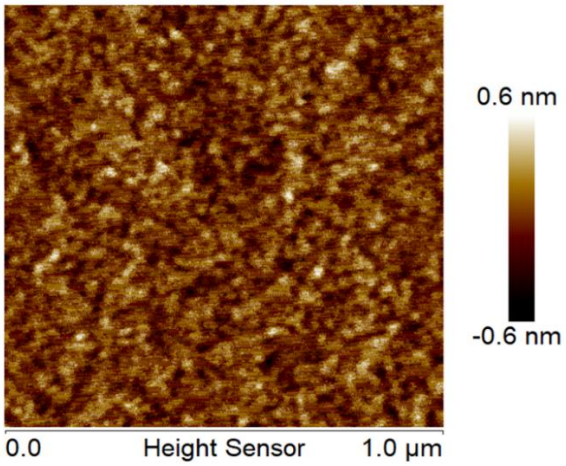

Figure 3.3. AFM of a-IGZO on a Si/SiO_x Substrate. The rms roughness is 0.184 nm.

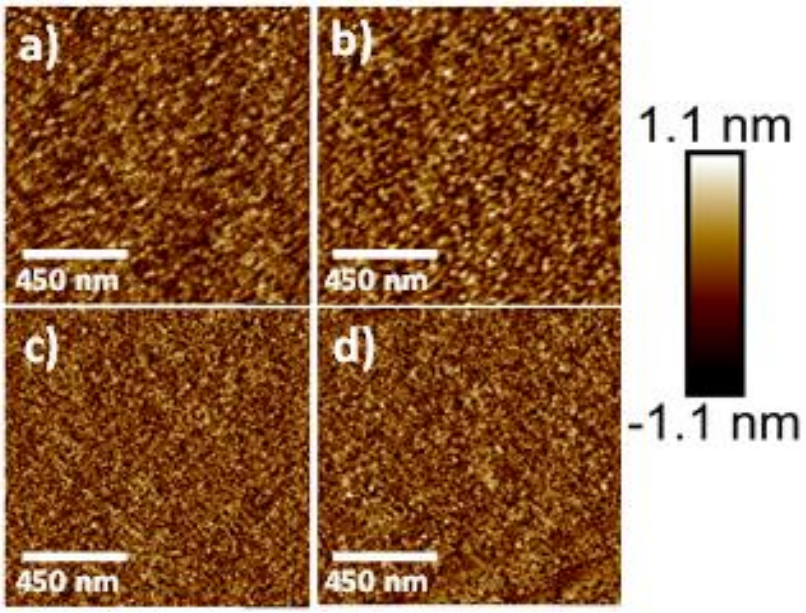

Figure 3.4. AFM Images of Hf-SAND Films on IGZO. (a) Hf-SAND-1 layer rms: 0.329 nm, (b) Hf-SAND-2 layer rms: 0.266 nm, (c) Hf-SAND-3 layer rms: 0.356, and (d) Hf-SAND-4 layer rms: 0.253 nm. Si substrates are used.

XRR (X-ray reflectivity) measurements, which provide film electron density profiles in the surface normal direction, were next used to evaluate the Hf-SAND film growth regularity on two layers of combustion-processed a-IGZO. The initial out-of-plane scattering data ($q = 4\pi \sin\theta/\lambda$) and the subsequent best fit model are shown in Figure 3.5a. The electron density profile was additionally normalized to the electron density of the underlying Si (ρ_{Si}) substrate (Figure 3.5b). The electron density profile in Figure 3.6 reveals the clearly defined alternating pattern of the lower and higher electron density regions in Hf-SAND-4 corresponding to the PAE and hafnia layers, respectively, as seen in previous SAND studies.[6–8] The appearance of the uniform periodic variations between organic and inorganic layers further demonstrates that SAND film growth has excellent regularity, which is not compromised by assembly on the a-IGZO surface. The capping hafnia layers and PAE layers are on average 1.05 and 1.08 nm thick, respectively, so that one bilayer is ∼2.13 nm. The primer HfO_x layer is about 1.82 nm thick, which is slightly thinner than might be expected. However, the exact thickness of the primer layer is difficult to determine as its electron density peak blends into that of the a-IGZO. The complete Hf-SAND-4 dielectric multilayer consisting of a primer layer and four bilayers (PAE/capping HfO_x) has a total thickness of ∼10.1 nm, which is slightly smaller than Hf-SAND-4 structures previously grown on Si substrates (∼13 nm).[6] From the electron density and thickness of the organic layers, the surface coverage is estimated to be ∼0.025 PAE molecules/$Å^2$, consistent with previous results on stilbazolium-based molecules self-assembled on Si/SiO_2.[34] PAE has a molecular length of ∼1.5 nm, which is larger than the experimental PAE layer thickness (1.08 nm), which reflects a PAE molecule tilt of ∼40° with respect to the surface normal, as found in other SAND derivatives.[8,9]

The XRR-derived interfacial roughnesses (~0.27−0.68 nm) are consistent with those determined by AFM (*vide supra*; Table 3.1).

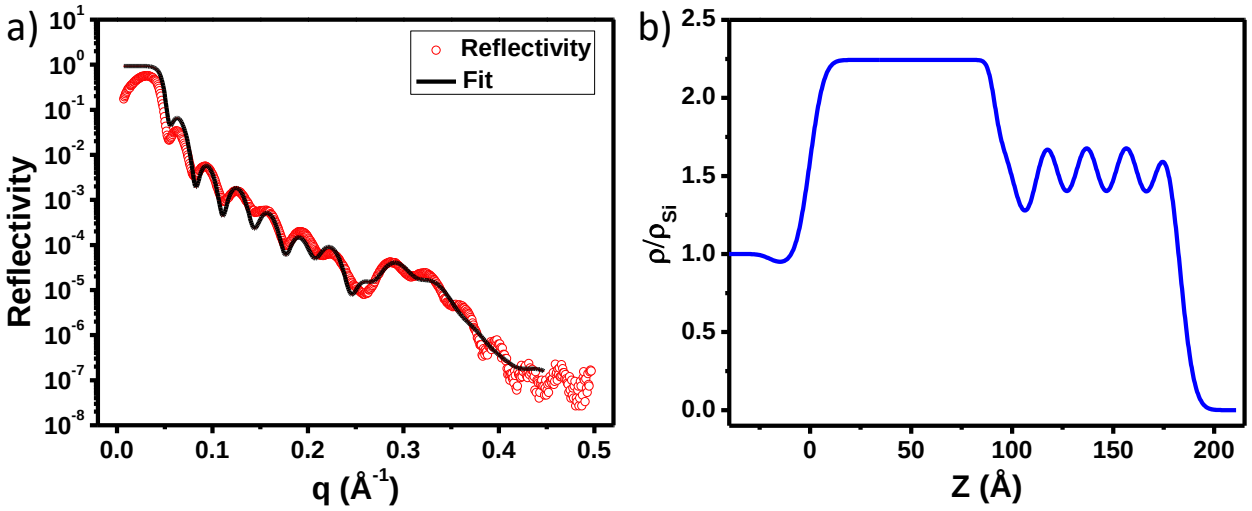

Figure 3.5. XRR Data and Si Normalized Profile for Hf-SAND-4 Grown on a-IGZO. a) XRR data with best fit shown in black. b) Si normalized electron density profile.

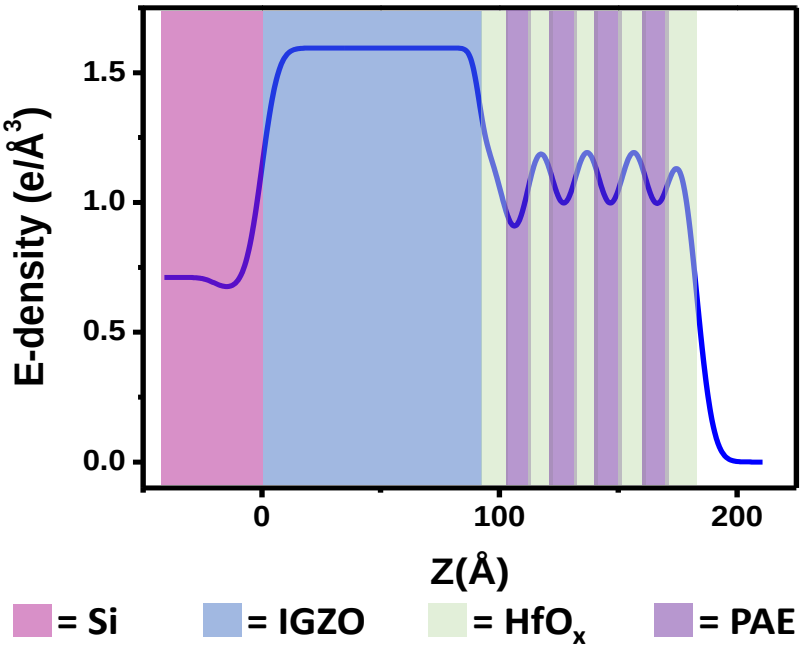

Figure 3.6. The XRR Electron Density Profile vs. Height (Z) Above the Si Surface of a-IGZO/Hf-SAND-4. The reflectivity data clearly show the growth of well-defined alternating hafnia and PAE layers. The primer hafnia layer blends into the electron density of the underlying a-IGZO. Note, two layers of a-IGZO were spin-coated onto a Si substrate for this experiment.

Table 3.1. XRR Derived Root-Mean-Square Roughness Data

Layer Interface	Roughness (Å)
SiO_2/IGZO	5.49
IGZO/Hf-Primer	2.67
Hf-Primer/PAE-1	5.63
PAE-1/Hf-Capping-1	6.77
Hf-Capping-1/PAE-2	5.93
PAE-2/Hf-Capping-2	6.77
Hf-Capping-2/PAE-3	5.93
PAE-3/Hf-Capping-3	6.77
Hf-Capping-3/PAE-4	5.93
PAE-4/Hf-Capping-4	6.77
Hf-Capping-4/Au	5.93

Lastly, CS-TEM imaging (Figure 3.7 and Figure 3.8a) elucidates the final top-gate TFT structure and the good quality of the a-IGZO/Hf-SAND interface. The bright area in the lower left corner corresponds to the SiO_2 substrate on which the TFTs were fabricated. Since the semiconductor is grown by combustion synthesis with multiple spin-coating/annealing steps to achieve film densification and the desired thickness,[9,35] the CS-TEM image clearly shows the multilayer character of the a-IGZO structure. In the Hf-SAND region, the alternating layers of low and high scattering contrast corresponding to the HfO_x and PAE layers, respectively, are also clearly visible (Figure 3.7). However, SAND is more sensitive to beam damage, so the layers are not as well defined as those in a-IGZO. Based on CS-TEM, the approximate thicknesses of the Hf-SAND-4 and a-IGZO (12 spin-coated) layers are 16 and 38 nm, respectively. These thicknesses are both in the expected range for the respective layers, thus further confirming the regular SAND growth on a-IGZO. Hf-SAND-4 is thicker in CS-TEM than XRR (~16 nm vs ~10.1 nm). This is likely due, in part, to the differences in the TFT substrate used for CS-TEM and the Si/a-IGZO substrate used for XRR. For the CS-TEM substrate, the contacts and a-IGZO were already fabricated and patterned when the Hf-SAND was deposited. Therefore, the HfO_x layers in the final TFT sample are at a greater distance from the annealing heat source, potentially resulting in slightly less oxide layer densification. Again, the full thickness of the primer HfO_x layer is difficult to determine from XRR due to the blending of the a-IGZO electron density with that of the HfO_x primer layer.

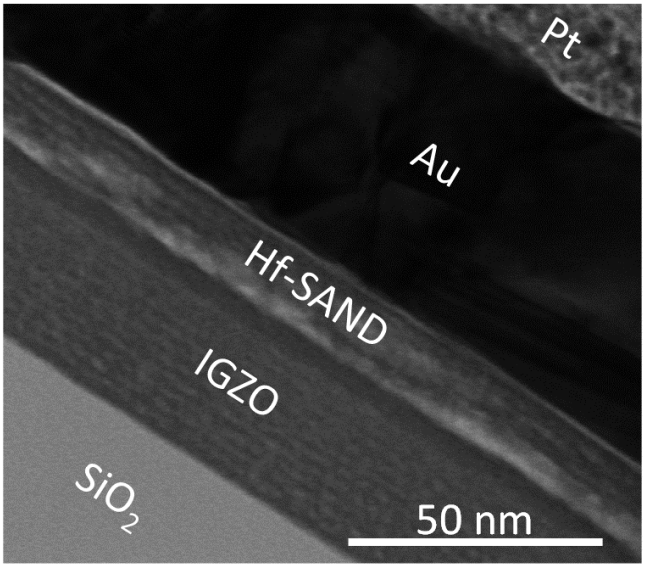

Figure 3.7. CS-TEM Image of a Completed Top-Gate a-IGZO/Hf-SAND-4 TFT. The gate electrode (gold), the dielectric (Hf-SAND), the semiconductor (a-IGZO), and the SiO_2 substrate are shown.

The identities of the Hf-SAND-4 layers were further confirmed by energy-dispersive spectroscopy (EDS) mapping, revealing that In, Hf, and Au are present in the expected regions. The lighter elements Zn, Ga, and Si are more dispersed but are detected in the anticipated areas (Figure 3.8b−h). Therefore, it is confirmed that Hf-SAND growth on solution-processed a-IGZO is eminently feasible with no significant differences versus growth on thermal Si/SiO_x substrates.

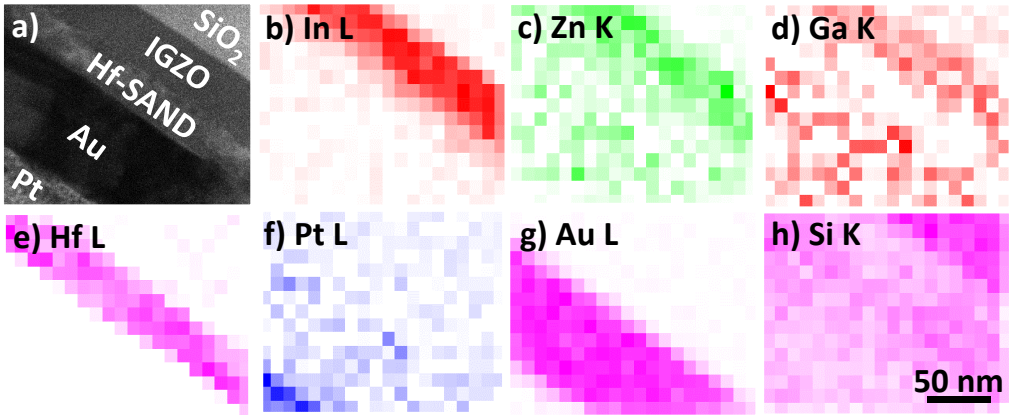

Figure 3.8. EDS Elemental Mapping of a-IGZO/Hf-SAND-4 TFTs. EDS elemental mapping images of (b) indium, (c) zinc, (d) gallium, (e) hafnium, (f) platinum, (g) gold, and (h) silicon of the CS-TEM image of top gate SAND TFT (a).

3.3.3 SAND Electrical Characterization

Before performing transport measurements on top-gate TFTs, the dielectric characteristics of the Hf-SAND-4 multilayers were assessed in metal−insulator−metal (MIM) capacitors. MIM devices were fabricated on ITO (bottom electrode) substrates with thermally evaporated gold contact pads (200 μm × 200 μm, top electrode) on the Hf-SAND-4 films. The capacitance and leakage properties were evaluated using a two-point probe station with a Signatone "cat-whisker" tungsten probe on the contact pads. To obtain accurate capacitances for Hf-SAND-4, it was essential to prepare MIM device structures as opposed to the metal−insulator−semiconductor (MIS) structures used in previous Hf-SAND studies.[6] The latter capacitance value is limited by the native SiO_x layer especially if the Si substrate is not in complete accumulation within the voltage range of the measurement.[5] The Hf-SAND-4 on ITO samples exhibit a capacitance of 732 ± 45 nF/cm^2 at 2.5 V (Figures 3.9 and 3.10a), which is higher than that previously reported for Hf-

SAND-4 on Si (610 nF/cm^2) due to the limiting effects of the substrate.[6] The k_{eff} value for Hf-SAND-4 on ITO fabricated here is 13.89. An additional advantage of Hf-SAND on ITO, and thus the similar environment of the present top-gate TFT structure as well, is that the Hf-SAND-4 capacitance varies by only ~8% (65 nF/cm^2) over a −3 to 3 V range. Capacitance vs. frequency (C-f) measurements show a gradual decline in capacitance as the frequency increases with a sharp drop near 10^6 Hz (Figure 3.11). The capacitance averages were 845 nF/cm^2 at 1 kHz, 759 nF/cm^2 at 10 kHz, and 708 nF/cm^2 at 100 kHz. Leakage current densities (J−V) were also measured for the MIM devices. The leakage current at 2 MV/cm is 7.41×10^{-7} A/cm^2. While at the extremes of the bias window (−2.97 to 2.97 MV/cm), the leakage current densities are in the low-10^{-6} A/cm^2 range, consistent with previous Hf-SAND-4 devices (Figures 3.10b and 3.12 and Table 3.2).[6] Considering the large contact pads, especially when compared to the dielectric thickness used in these measurements, it is evident that Hf-SAND-4 fabricated on ITO is essentially pinhole-free and of high quality.

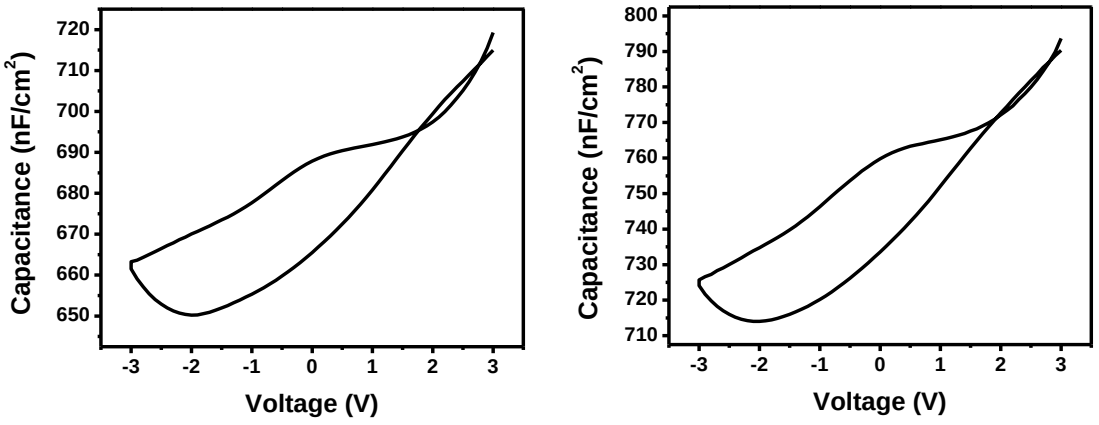

Figure 3.9. Representative Capacitance vs. Voltage Plots for Hf-SAND-4. The Hf-SAND-4 films were grown on ITO.

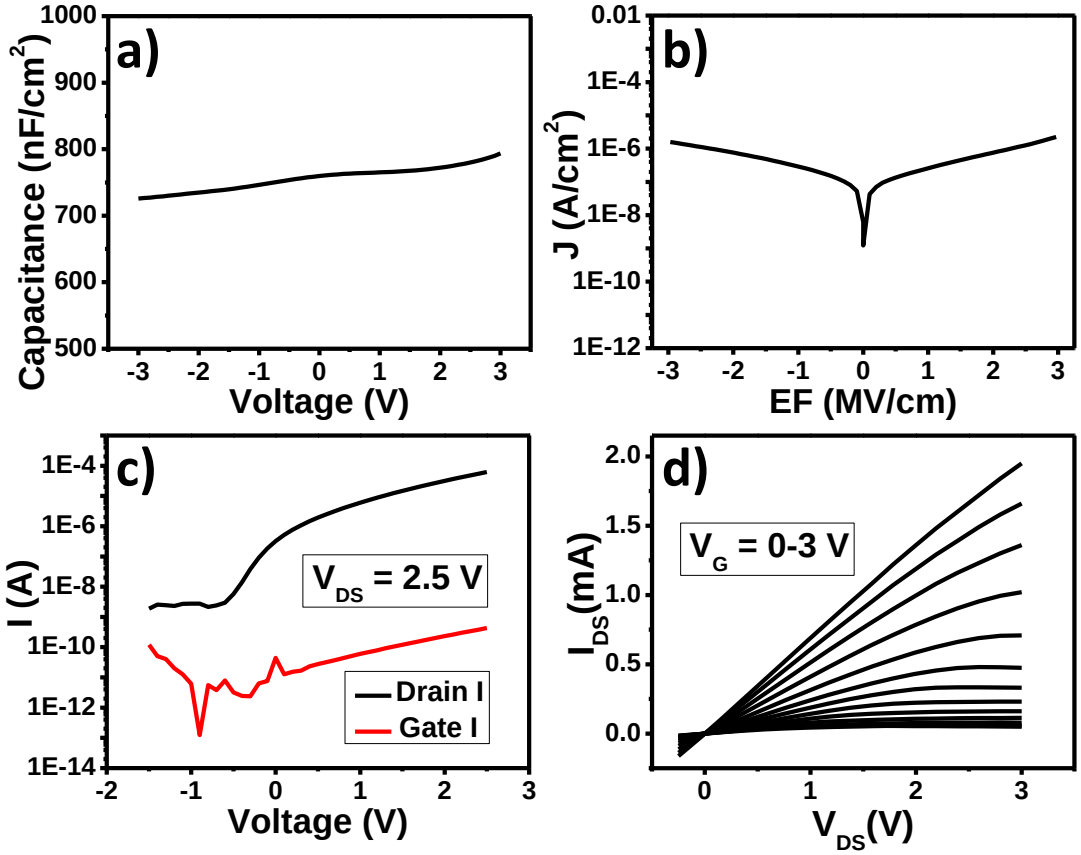

Figure 3.10. Plots of Dielectric Measurements on Hf-SAND-4 and Transistor Measurements on a-IGZO/Hf-SAND-4 TFTs. a) Representative capacitance plot at 10 kHz and b) leakage current of Hf-SAND-4 on ITO. c) Log transfer and d) output plots for top-gate a-IGZO/Hf-SAND-4 TFTs.

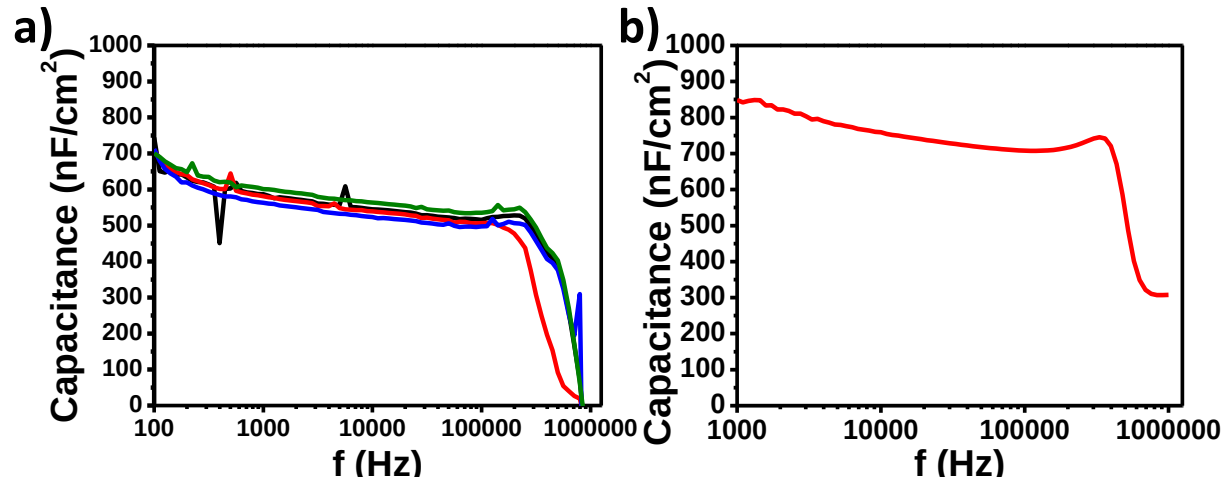

Figure 3.11. Representative Capacitance vs. Frequency Plots for Hf-SAND-4 on ITO. a) Frequency from 10^2 to 10^6 Hz and b) average of the measurements taken from 10^3 to 10^6 Hz. The capacitances listed in the main text in regards to C-f data were taken from the average data obtained on an Agilent B1500A (as shown in plot b).

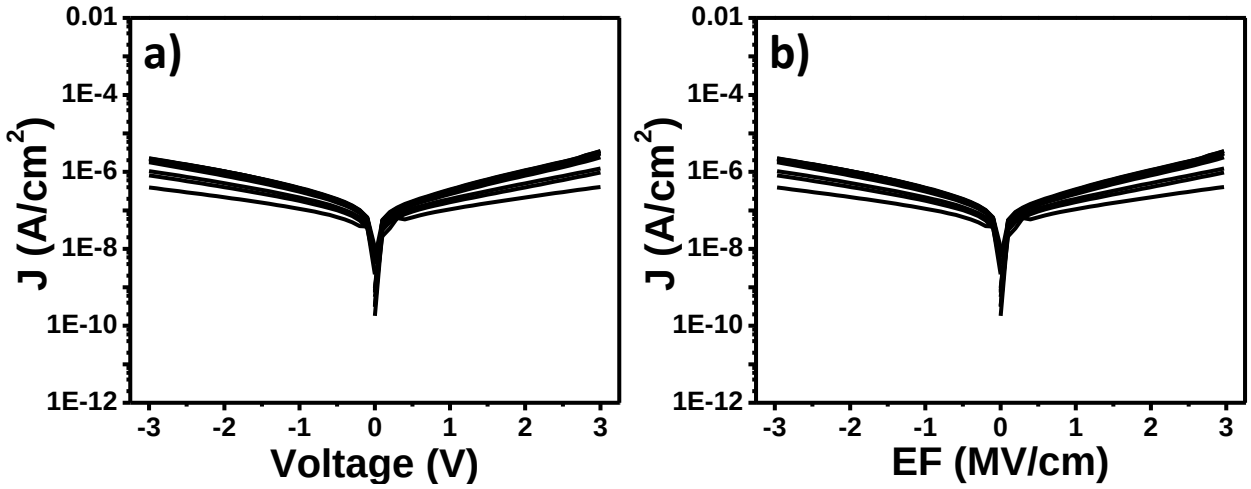

Figure 3.12. Representative Leakage Plots for Hf-SAND-4. a) Leakage vs. voltage and b) leakage vs. electric field plots for Hf-SAND-4 multilayers self-assembled on ITO.

Table 3.2. Leakage Data for Hf-SAND-4 Self-Assembled on ITO at Various EF Values

EF (MV/cm)	Leakage (A/cm^2)
-2.97 (also -3 V)	1.58×10^{-6}
2.97 (also 3 V)	2.23×10^{-6}
-2.5	1.10×10^{-6}
2.5	1.23×10^{-6}
-2	7.44×10^{-7}
2	7.41×10^{-7}

Next, the top-gate a-IGZO/Hf-SAND-4 TFT (L = 50 μm, W = 150 μm) properties were evaluated. The TFT I−V curves (Figure 3.10c and Figure 3.12) exhibit the expected linear and saturation behavior. Using an Hf-SAND-4 on ITO capacitance value of 732 nF/cm^2, the average saturation electron mobility is found to be 19.4 ± 0.5 cm^2 V^{-1} s^{-1}. The small variance in the capacitance from −3 to 3 V means that the mobility varies by less than 6% for the entire capacitance range. The most direct comparison for the top-gate TFT materials presented here is previous work using Hf-SAND-4 and printed combustion-processed a-IGZO in a bottom-gate top-contact device geometry.[13] In both sets of devices, a-IGZO was annealed at 300 °C. Note that the previous bottom-gate devices were unpatterned and had a (common) doped Si bottom gate and Al as the top source/drain contacts. The average saturation mobility of the printed devices, 20 cm^2 V^{-1} s^{-1}, is very similar to that achieved in the current work and further demonstrates the integrity of both the solution-processed a-IGZO and Hf-SAND-4 in a top-gate device configuration, despite the more complex fabrication process.[13] For the present top-gate a-IGZO/Hf-SAND-4 devices, the average threshold voltage (V_{th}) is 0.83 ± 0.04 V, and the small operating voltage range (−1.5 to 2.5 V) is suitable for most technological applications.[6,8,13,36] The present TFTs also exhibit low gate leakage currents with maxima in the mid-10^{-10} A range. The average log(I_{on}:I_{off}) and SS for the top-gate

devices are 4.26 ± 0.31 and 293 ± 22 mV/dec, respectively. The SS was calculated from the following equation:

$$SS = \frac{\partial V_g}{\partial(log_{10}\, I_D)}$$

where V_g is the gate voltage and I_D is the drain current.

In a-IGZO films, oxygen vacancies and other defects play a significant role in device performance.[37,38–40] Studies of a-IGZO films indicate that the role of oxygen vacancies and trap densities is highly dependent on growth conditions such as O_2 partial pressure and annealing parameters; the density of defects is expected to be higher in solution-processed films and their effects more evident.[38,39] Note that often the dielectric leakage current dictates the off current of a device. In the present case, the top-gate a-IGZO/Hf-SAND-4 TFT off current is a few orders of magnitude greater than the leakage current (Figures 3.10c and 3.12), indicating significant defects. The layered structure of a-IGZO seen in the cross-sectional TEM (Figure 3.8) seems to indicate that there is variation in the oxide throughout the semiconductor. This could be due to the differing exposure of the layers to ambient during processing and is potentially a source of bulk trap states; however, further investigation will be necessary to determine the extent and nature of the effects.[18,41]

The subthreshold slope depends on both the bulk trap density (D_{bulk}) and the trap density of the interface (D_{it}). The D_{it} was calculated using the following equation:

$$D_{it} = \frac{C_i}{e^2}\left(\frac{eSS}{k_B T \ln(10)} - 1\right)$$

where C_i is the geometric capacitance of the dielectric, *e* is the elementary charge, SS is the subthreshold slope, k_B is the Boltzmann constant, and T is the temperature. This calculation of the trap density assumes that $D_{bulk} = 0$. As noted above, the presence of bulk trap states is expected in both sputtered and solution-processed a-IGZO. Regardless, this estimation of D_{it} gives an indication of the interfacial trap density. Comparing the trap densities of the present Hf-SAND devices and other a-IGZO TFTs from the literature indicates that Hf-SAND devices tend to have a slightly higher trap density (1.18×10^{13} eV^{-1} cm^{-2}) than most comparable devices (Table 3.3). Higher D_{it} versus other devices in literature is not necessarily unexpected as the top-gate Hf-SAND-4 TFTs fabricated here are the first examples where both the semiconductor and dielectric were solution-processed.

Table 3.3. Fabrication and Trap Density Comparison from Literature

a-IGZO Deposition Method	Dielectric Deposition Method	Dielectric Material	SS (mV/dec)	D_{it} (eV^{-1} cm^{-2})
RF Sputtering	PECVD	SiN_x	430	~7.4E+11[42]
RF Sputtering	ALD	Al_2O_3	360[43]	1.14E+12
RF Sputtering	Spin Coating	P(VDF-TrFE)	275[44]	1.85E+13
DC Sputtering	Spin Coating	ZeoCoat	190[20]	1.16E+11
-	ALD/PECVD	Al_2O_3/SiN_x	170[19]	4.35E+11
RF Sputtering*	RF Sputtering	SiO_2	116.1	4.2E+11[45]
RF Sputtering	Spin Coating	Siloxane	320±100	2.23E+11[46]
Spin Coating	Spin Coating	Hf-SAND	293±22	1.81E+13

= Top-Gate Top-Contact Structure *Semiconductor included a buried ITO layer

The interfacial trap density also has a significant impact on the hysteresis of a TFT. The hysteresis seen in the a-IGZO/Hf-SAND-4 devices (Figure 3.13) is in the anticlockwise direction, which is unusual since a-IGZO device hysteresis is typically in the clockwise direction.[37] In previous work using combustion-processed IGZO, clockwise hysteresis was observed.[18] However, the anticlockwise hysteresis behavior is also seen in the bottom-gate printed a-IGZO devices on Hf-SAND-4, implying that the hysteresis is dominated by interactions with the Hf-SAND.[13] A threshold voltage shift (ΔV_{th}) of 1.86 V in the negative direction is observed between the forward and reverse sweeps of the top-gate TFTs, which is somewhat larger than that seen in the printed a-IGZO/Hf-SAND-4 bottom-gate devices (Figure 3.13).[13] This is expected as the more complex fabrication process required for the top-gate devices may create more interfacial states. Additionally, spin-coated combustion-processed semiconductors are known to be porous, particularly in the last layer applied, which is generally beneficial in the bottom-gate architecture as successive layers can fill in the pores and potential defects of the previous layers.[10,18] In the case of these top-gate devices, however, the last IGZO layer applied is that which forms the interface with the dielectric, and thus the porosity might be a source of traps. Further optimization of these promising devices should result in lowering the bulk and interfacial trap densities.

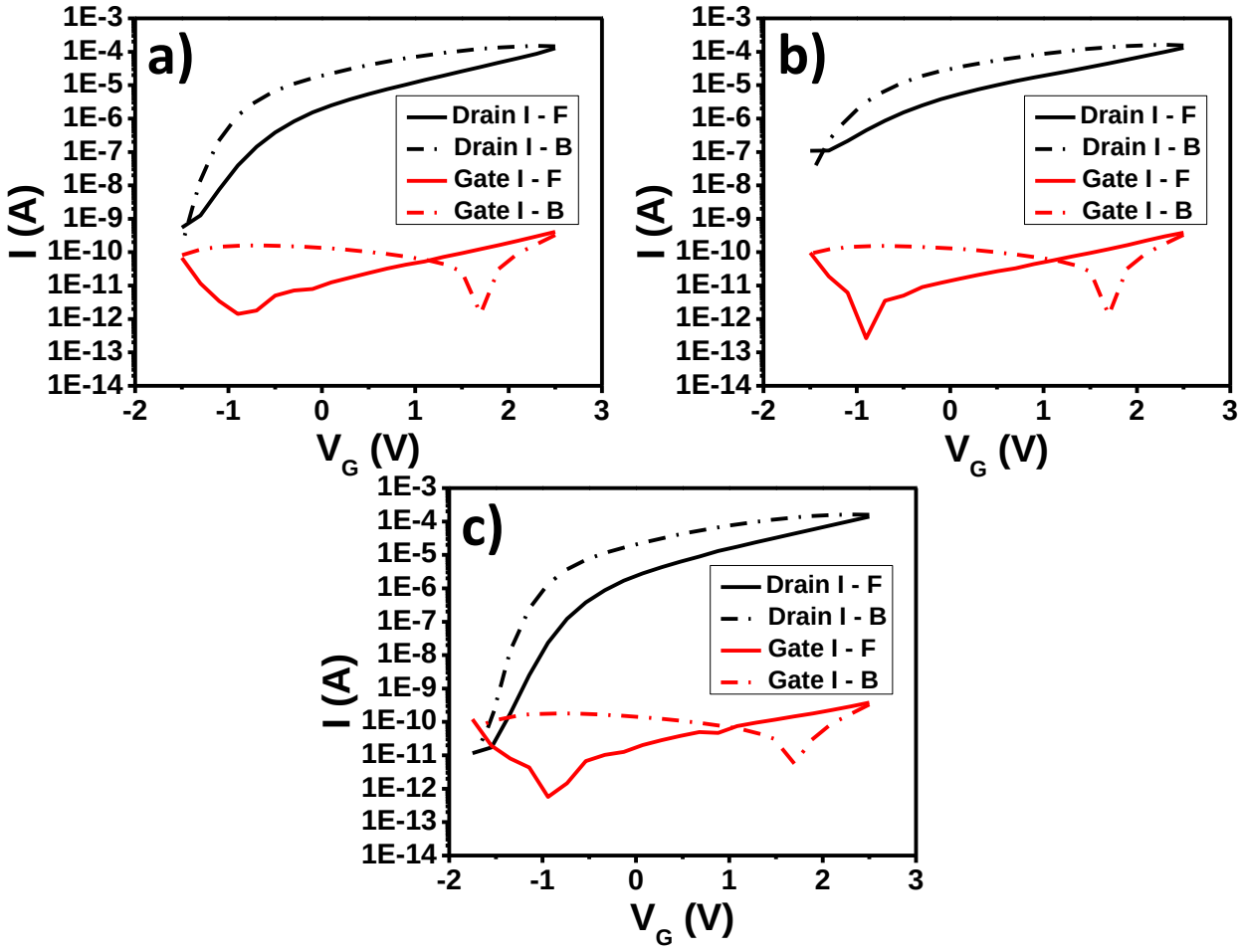

Figure 3.13. Log Transfer Plots of Top-Gate a-IGZO/Hf-SAND-4 TFTs with Forward and Reverse Sweeps. The forward sweeps are shown as solid lines and the reverse sweeps as dotted lines (a, b, and c).

3.3.4 a-IGZO-SAND TFT Performance Comparison with the Literature

For greater context regarding IGZO top-gate devices, the a-IGZO/Hf-SAND-4 TFTs are compared to literature examples in Figure 3.14 and Tables 3.4 and 3.5. The highest mobility for top-gate IGZO transistors in the literature is 44.57 $cm^2\ V^{-1}\ s^{-1}$ reported by Hsieh et al.[42] These devices were fabricated with a 300 nm SiN_x dielectric and IGZO layers deposited via plasma-

enhanced chemical vapor deposition and RF sputtering, respectively.[42] Another impressive mobility of 39.9 $cm^2 V^{-1} s^{-1}$ was reported for devices fabricated with a plasma-enhanced atomic layer deposited SiO_2 dielectric and sputtered IGZO.[47] Additional large literature mobilities are 35.6, 26, 22, and 21.20 $cm^2 V^{-1} s^{-1}$ produced by top-gate top-contact (TG-TC) devices with 10 nm RF sputtered SiO_2 and a buried ITO layer in a-IGZO via RF sputtering, TG-BC devices with a sputtered SiO_x/SiN_x dielectric, TG-TC transistors utilizing a 250 nm spin-coated siloxane dielectric, and coplanar contact devices with a 150 nm SiO_x dielectric, respectively.[45,46,48,49] All of the aforementioned devices used sputtered IGZO. Impressively, the present Hf-SAND devices yield the seventh highest mobility (μ_{SAT} = 19.4 $cm^2 V^{-1} s^{-1}$) out of the 31 literature examples while being the only TFTs fabricated from both solution-processed dielectric and semiconductor layers.

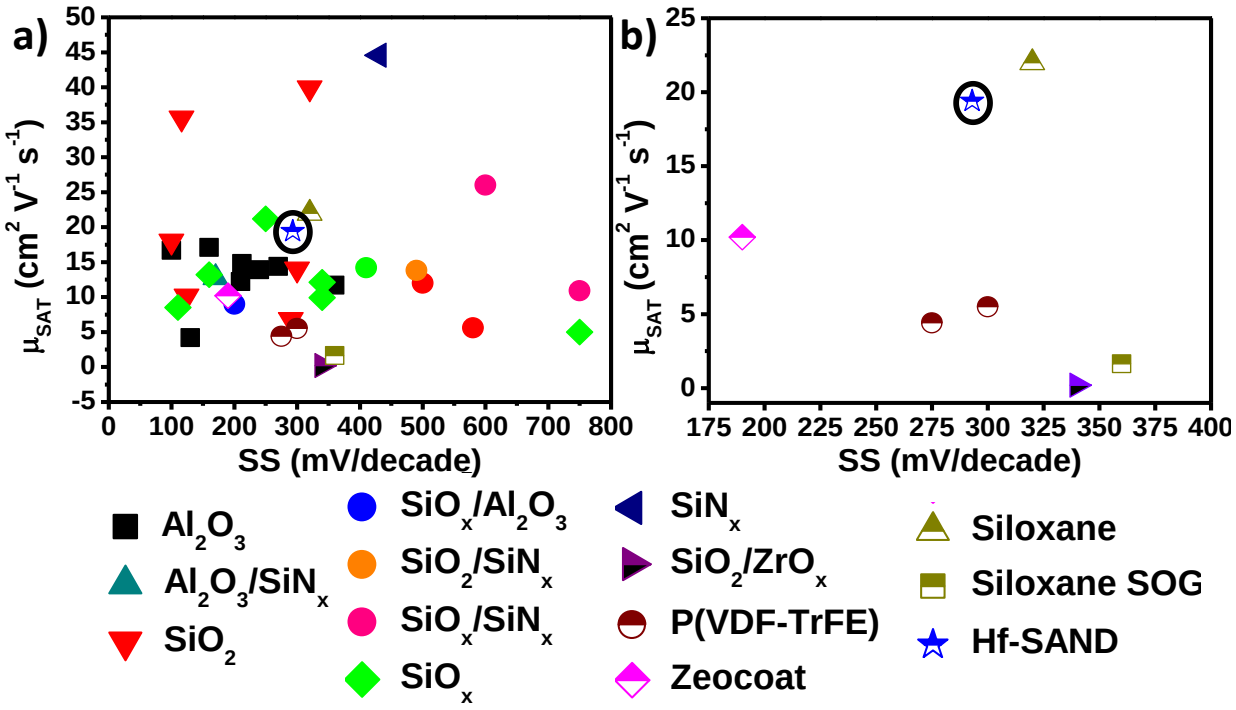

Figure 3.14. Plots of Mobility vs. SS of Top-Gate IGZO TFTs from the Literature. a) Mobility vs. subthreshold slope (SS) of literature top-gate IGZO TFTs for various dielectric materials.[19,20,42-70] b) Mobility vs. SS for IGZO TFTs with solution-processed dielectrics. The circular symbols represent linear mobilities. Symbols that are partially filled indicate solution-processed dielectrics. The black circles designate solution-processed semiconductors. See Tables 3.4 and 3.5 for more complete fabrication information and literature TFT metrics.

Table 3.4. Top-Gate a-IGZO TFTs with Vapor Deposited Dielectric Metrics from the Literature

Dielectric Thickness (nm)	Dielectric Deposition Method	Dielectric Material	Semiconductor Deposition Method	μ_{SAT} ($cm^2 V^{-1} s^{-1}$)	V_{th} (V)	SS (mV/decade)
185	ALD	Al_2O_3	RF Sputtering	14.8	1.8	212[50]
185	ALD	Al_2O_3	Sputtering	12.2	1.73	210[51]
150	ALD	Al_2O_3	RF Sputtering	16.7	-0.3	100[52]
190	ALD	Al_2O_3	RF Sputtering	11.7	-	360[43]
50	ALD	Al_2O_3	Sputtering	4.2	1	130[53]
110	ALD	Al_2O_3	RF Sputtering	14.4	0.74	270[54]
112	ALD	Al_2O_3	RF Sputtering	17.1	-	160[55]
80	ALD	Al_2O_3	Sputtering	13.9	-1.03	240[56]
30/120	ALD/PECVD	Al_2O_3/SiN_x		12.8*	-0.7#	170[19]
15/15	PECVD/ALD	SiO_x/Al_2O_3	Sputtering	9*	2.2	200[57]
300	PECVD	SiN_x	RF Sputtering	44.57	1.91	430[42]
50/300	PECVD	SiO_2/SiN_x	RF Sputtering	13.8*	2.6	490[58]
50/300	PECVD	SiO_x/SiN_x	RF Sputtering	10.9*	0.9	750[59]
	PECVD	SiO_x/SiN_x	RF Sputtering	26*	0.1	600[48]
300	PECVD	SiO_x	RF Sputtering	5.01	-0.98	750[42]
200	AKT PECVD	SiOx	PVD	13.2	0.10	160[60]
200	PECVD	SiO_x	DC Magnetron Sputtering	9.9	1.41	340[61]
200	PECVD	SiO_x	DC Sputtering	14.2*	0.22	410[62]
		SiO_x		12.13	2.55	340[61]
-	PECVD	SiO_x	DC Sputtering	8.5	0.8	110[63]
150	PECVD	SiO_x	Sputtering	21.2	-0.56	250[49]
50/300	PECVD	SiO_2/SiO_2	RF Sputtering	5.6*	4.9	580[58]
-	PEALD/PECVD	SiO_2	Sputtering	39.9	-1	320[47]
8.62	PECVD	SiO_2	DC Magnetron Sputtering	10.13	0.52	124[64]
200	PECVD	SiO_2	Sputtering	~14	0.5#	~300[65]
100	PECVD	SiO_2	Sputtering	6.8		290[66]
200	CVD	SiO_2	DC Sputtering	10.0-12.0*	-	500[67]
200	RF Sputtering	SiO_2	RF Sputtering	18	-1.35	100[68]
10	RF Sputtering	SiO_2	RF Sputtering	35.6	1.3	116.1[45]

= Top-Gate Top-Contact Structure #Indicates V_{on} *Indicates linear mobility

Table 3.5. Top-Gate a-IGZO TFT with Spin-Coated Dielectric Device Metrics from Literature

Dielectric Thickness (nm)	Dielectric Deposition Method	Dielectric Material	Semiconductor Deposition Method	μ_{SAT} ($cm^2\ V^{-1}\ s^{-1}$)	V_{th} (V)	On/Off Ratio	SS (mV/decade)
10/65	PECVD/Spin Coating	SiO_2/ZrO_x	RF Sputtering	0.2	0.3	1.00E+03	340[69]
60	Spin Coating	P(VDF-TrFE)	RF Sputtering	5.5*	-	1.15E+08	300[44]
110	Spin Coating	P(VDF-TrFE)	RF Sputtering	4.4*	-	2.50E+08	275[44]
400	Spin Coating	Zeocoat	Sputtering	9.8	-1.3		190[20]
250	Spin Coating	Siloxane	RF Sputtering	22	5.6	1E+06	320[46]
360	Spin Coating	Siloxane SOG	RF Sputtering	1.64	1.82		360[70]
10.1	Spin Coating	Hf-SAND	Spin Coating	19.4	0.83	1.80E+04	293

= Top-Gate Top-Contact Structure *Indicates linear mobility

The performance of the present Hf-SAND transistors is impressive in the context of all reported top-gate IGZO devices, but especially so in comparison with TFTs with spin-coated dielectrics. Lee et al. reported TG-TC RF sputtered a-IGZO devices with a spin-coated 110 nm poly(vinylidene fluoride-trifluoroethylene) [P(VDF-TrFE)] dielectric, having a linear mobility of 5.5 $cm^2\ V^{-1}\ s^{-1}$. The P(VDF-TrFE) layer is >10× thicker than the Hf-SAND dielectric but has higher leakage currents, 2.2×10^{-6} A/cm^2 at 2 MV/cm and 7.41×10^{-7} A/cm^2 at 2 MV/cm, respectively.[44] Zeocoat, another polymer dielectric, was used by Toda et al. to produce TG-TC transistors with DC magnetron-sputtered IGZO, where the mobility was 9.8 $cm^2\ V^{-1}\ s^{-1}$ and the V_{th} was −1.3 V.[20] The highest mobility for a solution-processed dielectric with a sputtered IGZO film was 22 $cm^2\ V^{-1}\ s^{-1}$ reported by Kulchaisit et al. These devices had a TG-TC structure with RF magnetron-sputtered a-IGZO and a spin-coated siloxane dielectric. The siloxane devices

additionally had a V_{th} of 5.6 V, a SS of 320 ± 10 mV/decade, and an I_{on}:I_{off} of ~10^6. The 250 nm-thick siloxane layer had gate leakage currents comparable to the ~16 nm Hf-SAND during TFT operation.[46] However, the siloxane layer required annealing at 300 °C - 100 °C higher than that for Hf-SAND. Thus, the combination of combustion-processed a-IGZO and Hf-SAND-4 in TG-BC TFTs yields impressive mobilities versus all previous top-gate IGZO TFTs, especially those with solution-processed dielectrics, and is the only example in the peer-reviewed literature of solution-processed semiconductor + solution-processed dielectric pairing. These results are therefore especially significant given the general desire for the manufacturing of optoelectronic devices to transition from capital-intensive vapor deposition techniques to more cost-effective solution-based ones.[1–4] In addition to the results presented here, the potential use of solution-processed SANDs in manufacturing is further strengthened by the recent development of printed SANDs.[16]

The well-known sensitivity of a-IGZO to atmospheric effects is known to contribute to device instability and is a major attraction of top-gate devices.[37,45,54] Numerous studies have reported improved environmental stability of top-gate a-IGZO TFTs using a variety of dielectric materials.[40,42,46,47] It is therefore expected that the top-gate SAND TFTs will have superior environmental stability compared to bottom-gate devices. A further advantage of the solution-processed Hf-SAND used here is limiting a-IGZO damage by high-energy dielectric deposition techniques such as sputtering.[19,47,69] The confirmed viability of SAND in top-gate TFT structures also opens possibilities for further work on SAND-based device durability, such as long-term stability testing, an important step for deeper understanding of the properties of this unconventional hybrid dielectric.

3.4 Conclusions

This investigation demonstrates that Hf-SAND gate dielectrics can be successfully self-assembled from solution in top-gate TFT architectures using combustion-processed a-IGZO as the underlying channel layer. Characterization of Hf-SAND films grown on a-IGZO via UV−Vis spectroscopy, AFM, XRR, and CS-TEM demonstrates that the robust, regular SAND nanostructure is preserved under the processing conditions required for top-gate TFT fabrication. These solution-processed a-IGZO/Hf-SAND top-gate devices exhibit impressive mobilities of 19.4 $cm^2\ V^{-1}\ s^{-1}$ with low (< 1V) operating voltages, low gate leakage currents (10^{-10} A), and a good SS of 293 mV/dec. As SANDs have already shown extensive durability and versatility in terms of well-matched semiconductors, this newly confirmed compatibility with top-gate structures further expands the uses and applications of this effective unconventional dielectric family.

Chapter 4

Processing, Structure, and Transistor Performance: Combustion versus Pulsed Laser Growth of Amorphous Oxides

4.1 Background

For optoelectronic technologies, amorphous transparent conducting oxides (a-TCOs) offer many attractions over their crystalline counterparts. Their amorphous nature ensures a lack of grain boundaries, making a-TCOs well-suited for large area applications.[1,2] Of even greater importance, amorphous oxides (a-oxides) can be grown at low temperatures as semiconductors with high mobility and have demonstrated excellent thin-film transistor (TFT) device performance when grown near room temperature.[3–5] Low temperature depositions afford lower processing costs and, more notably, enable the use of flexible polymeric substrates.[6,7] Flexible electronics offer the promise of more durable, portable, and biocompatible devices for the increasingly ubiquitous personal electronics industry.[8–10]

Solution-processing offers the potential of high-throughput roll-to-roll printing and patterning of flexible electronics, increasing the large-scale manufacturability of amorphous oxide films.[10] However, the realization of high-quality/high-mobility amorphous oxide films on flexible substrates was initially hindered by the requirement of high synthesis temperatures ($\geq$ 400°C) in more traditional sol-gel methodologies, and the thermal limit of low-cost flexible substrates is <350°C.[11–13] Recent work has demonstrated that amorphous metal oxide (a-MO) films can be fabricated via solution-processing methods at low temperatures.[4,14–16] Low substrate temperatures can be maintained during growth and densification by introducing additional energy into the film growth precursors through simultaneous UV irradiation[7,17,18] or solution-based fuels, resulting in good device-quality films.[19–22] Combustion synthesis is one of the most promising low-temperature solution-processing methods.[20] Combustion synthesis creates small, local-scale, exothermic reactions through the addition of acetylacetone or other “fuels” into metal nitrate

precursor solutions.[20,22] These local-scale reactions effectively lower the activation barrier to metal oxide lattice condensation and reduce the global annealing temperature.[20,22] Combustion synthesis (CS) solutions can be deposited onto substrates through either a spray (Spray-CS, Figure 4.1B)[23,24] or spin (Spin-CS, Figure 4.1C)[20,21,25] coating process. Spray-CS is particularly well suited for uniform large-area production.[24] However, to date most fundamental understanding of a-MO films is derived from studies of films grown by physical vapor deposition (PVD) techniques, such as sputter deposition and pulsed laser deposition (PLD). These methods are quite different from combustion synthesis because PVD a-oxide growth methods lack solvent and air exposure, and do not require heating.

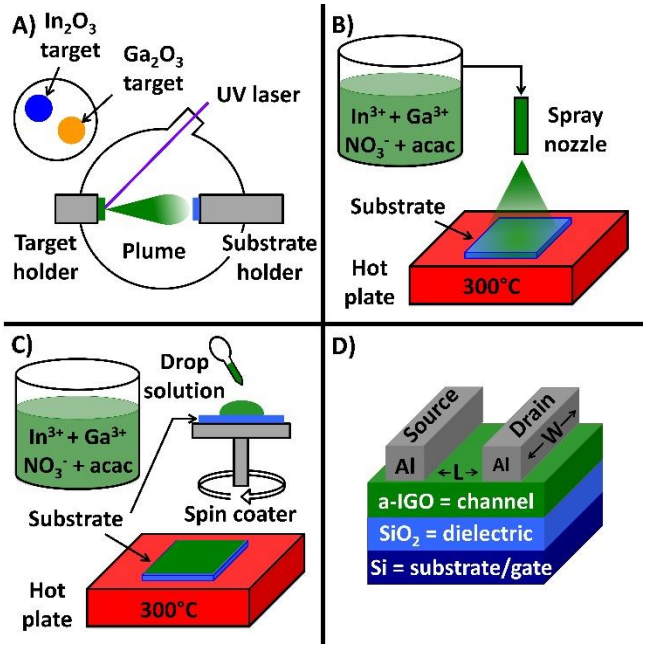

Figure 4.1. Schematic Illustrating the Depositions Methods of IGO Films and BG-TC TFT Structure. A) PLD method, B) Spray-CS method, and C) Spin-CS method. All three film growth methods were used in creating the channel layer in thin-film transistors with the bottom-gate top-contact (BG-TC) architecture shown in D).

Significant advances can be made in controlling a-oxide performance by understanding how processing parameters influence film structure. In the field of a-TCOs, important strides have been made in linking processing metrics, such as cation ratios,[26,27] deposition temperature,[28,29] and oxygen content,[30,31] with film structure to better understand performance. However, most of these studies focused on PVD methods which, unlike combustion synthesis, do not involve solvent or ambient air exposure. In this work a direct and in-depth comparison of pulsed laser deposition (PLD, Figure 4.1A) and combustion processing (spray and spin, Figures 4.1B and 4.1C) is performed to elucidate the effects of processing methodology on the microstructural properties and electronic performance of a-oxide semiconductors. Importantly, this direct comparison enables the extensive PVD literature of amorphous oxides to be leveraged in building an understanding of the emerging CS growth technique. This comparison is made using the amorphous indium gallium oxide (a-IGO) system as a model a-MO class. The use of a materials system rather than a single composition enables the systematic comparison of structure-property trends and provides greater confidence in assessing the underlying causes. Furthermore, utilizing only one modifying cation, Ga, negates the competing effects of multiple cations seen in previous studies of multication systems, such as indium gallium zinc oxide (In-Ga-Zn-O).[1,23,24,32] A foundational study exploring Ga as a modifying cation in a-IGO PLD will be referenced when understanding the Ga-dependent trends in this work.[27] TFT performance is evaluated in devices fabricated on SiO_2/Si substrates with Al contacts and a-IGO channel layer films prepared by PLD, Spin-CS, and Spray-CS (Figure 4.1D).

Field effect mobility and threshold voltage are both important TFT performance metrics. High field effect mobility is important for creating TFTs capable of operating at high speeds and

enabling devices with fast refresh rates. Control of the threshold voltage (V_{th}) is important for improving the energy efficiency of transistors. An ideal transistor can be turned on at a low voltage and does not require a back-voltage to remain in the off state. Field effect mobility and V_{th} are tied to the properties of the channel layer material. Semiconductor channel layers need to have fast carrier mobility to have good field effect mobility and an optimized carrier concentration to have a near-zero threshold voltage. Here, we investigate and compare the TFT performance metrics of devices fabricated with PLD, Spin-CS, and Spray-CS channel layers by leveraging previous PVD studies.[27,33–35] These previous PVD studies developed an understanding of how a-MO structure influences carrier concentration and carrier mobility. A drop in TFT field effect mobility and a rise in V_{th}, with increasing Ga content, are shown for both PLD and Spin-CS devices. X-ray absorption spectroscopy (XAS) measurements reveal that the mechanism is the disparate local structure around Ga, as opposed to around In, which disrupts both carrier mobility and carrier production.[27] In contrast, mobility and V_{th} for Spray-CS films are dominated by the processing method and cannot be tuned with composition. Local structure studies reveal that the Spray-CS growth technique results in high In-O coordination levels which explain the low carrier concentrations and resultant V_{th} behavior.

The sensitivity of a-IGO film thermal phase stability to deposition parameters is assessed here through *in situ* glancing incidence X-ray diffraction (GIXRD) measurements taken during air annealing studies. The need to ensure thermal stability of the amorphous phase was emphasized as early as Nomura's work in 2004.[3] Multiple studies have explored the thermal phase stability of a-TCO phases in response to post deposition annealing but only for PVD-derived films.[26,36–39] Previous work has shown that the onset of crystallization can greatly reduce carrier mobility[28,39]

and result in poor threshold voltage uniformity.[40] When used as TFT semiconductors, a-oxides are only a single layer within a multilayer stack. Therefore, thermal phase stability is important to maintain consistent film performance after additional layers are deposited. Insight into thermal phase stability is obtained here through X-ray reflectivity (XRR) and XAS measurements. It will be seen that the evolution of film density upon crystallization is greatest for the combustion-processed films and contributes to the superior resistance to crystallization of these films over PLD films.

4.2 Experimental Section

4.2.1 Film Growth

Films used for thin-film transistors (TFTs) were deposited on SiO_2/Si substrates purchased from WRS Inc. The SiO_2 layer was confirmed, via ellipsometry of a blank substrate, to be 300 nm thick and served as the dielectric layer. Films used for the crystallization study were deposited on ⟨100⟩ Si wafers purchased from WaferNet Inc. A single crystal substrate is important for ensuring that observation of the amorphous-to-crystalline transition is not obscured by excess background scattering or Bragg peaks. Films used for XAS studies were deposited on quartz substrates. All substrates were ~2 × 2 cm^2. Before film deposition, substrates were sonicated in 200-proof ethanol for 10 minutes and O_2 plasma cleaned for 5 minutes.

Pulsed Laser Deposition (PLD)

All pulsed laser depositions employed a 248 nm KrF excimer laser (Figure 4.1A). The laser was focused to a 1 × 3 mm^2 spot size and used to ablate the ceramic targets, creating a plume of

target material. A laser-pulse-duration of 25 ns and a beam energy of 220 mJ/pulse was used. The laser pulse frequency was 2 Hz. To prevent localized heating, the targets were rotated, and the laser beam was rastered radially. Various indium-to-gallium ratios were achieved through alternating ablation between an In_2O_3 target and a Ga_2O_3 target, both purchased from Super Conducting Materials Inc. During each In_2O_3/Ga_2O_3 cycle less than a unit cell of material (< 1 monolayer) was deposited to ensure mixing at the atomic-layer level. For TFTs, films were grown at room temperature in a 48.5 ± 0.5 mTorr O_2 environment. Oxygen pressure in the deposition chamber was automatically set with feedback from a Baratron pressure gauge. A convection pressure gauge was used to verify the oxygen pressure. A target-to-substrate distance of 60 mm was used, and the resulting films were 15-17 nm thick. For crystallization studies, films were grown at -25 °C in a 7.5 ± 0.5 mTorr O_2 environment. A target-to-substrate distance of 10 cm was used to produce 25-35 nm thick films.

Combustion Synthesis (CS)

For combustion synthesis all reagents were purchased from Sigma-Aldrich and used as received. The precursor solutions were prepared with $In(NO_3)_3 \cdot xH_2O$ and $Ga(NO_3)_3 \cdot xH_2O$ salts in 2-methoxythanol to produce 0.05 M solutions. After the salts were completely dissolved, acetylacetone (2:1 ratio acetylacetone: metal) and ammonium hydroxide (1:1 ratio NH_4OH: metal) were added. The solutions were stirred at room temperature and aged overnight. The precursor solutions were mixed in the desired ratios and stirred at room temperature for approximately 1-2 hours before use.

For Spray-CS (Figure 4.1B), substrates were heated to 300 °C for the duration of the spray coating. For the crystallization and XAS studies, a lower temperature of 250 °C was used to ensure all films were amorphous. The precursor solution was sprayed through an ultrasonic nozzle, held 7.5 cm above the substrate, at a rate of 0.5 mL/min. Total spray time was adjusted to create films with thicknesses of 9-16 nm for TFTs, 30-58 nm for crystallization studies, and 200-400 nm for XAS studies.

Spin-CS (Figure 4.1C) was performed inside a dry-box (RH ≈ 23%), and the precursor solutions were deposited dropwise onto clean substrates, using syringes fitted with 0.2 μm filters, and then spun at 3500 rpm for 30 seconds. After each spin-coated layer, the films were annealed in air for 20 minutes at 300 °C. A total of four layers were deposited to create ~10 nm thick films for use in TFTs. Exactly 14 layers were used to create ~30 nm thick films for XAS and crystallization studies.

4.2.2 Transistor Fabrication and Testing

TFTs were fabricated with 10-15 nm thick channel layers deposited by PLD, Spin-CS, or Spray-CS across a range of a-IGO compositions. Precautions were taken to eliminate as many variables between the devices as possible. Transistors were made and tested within weeks of each other in the same laboratory by the same researcher. All films were grown on the same SiO_2/Si substrates. After deposition, all films were patterned by etching with oxalic acid to produce film areas slightly smaller than the shadow masks used for contact deposition. For Spin-CS and Spray-CS, the etched films were annealed at 300 °C in low humidity (<5%) for 50 minutes. Aluminum contacts were deposited via thermal evaporation (rate of > 1 Å/s and pressure $<4 \times 10^{-6}$ Torr)

through shadow masks. The channel geometry had a width (*W*) of 1 mm and length (*L*) of 50 μm. Immediately before testing, PLD films were annealed at 300 °C in low humidity (<5%) for 45 minutes. The devices were tested in ambient conditions using an Agilent B1500A semiconductor analyzer.

4.2.3 Film Composition

X-ray fluorescence spectroscopy (XRF) was performed on each sample to verify the In/Ga atomic ratio achieved. This measurement was essential since film composition did not strictly follow the PLD pulse ratios or solution processing precursor ratios. The film compositions were always gallium-weighted and pulse/solution ratios had to be adjusted. Note that a similar trend has been observed previously.[41] The Ga K and In L fluorescence yields were corrected for the different absorption cross-sections and detector efficiency according to:

$$D = \frac{A}{B\ C} \qquad E = \frac{D_{Ga}}{D_{Ga} + D_{In}}$$

where A is the integrated area of the fluorescence peak, B is the XRF cross-section, C is the detector efficiency, D is the corrected peak intensity calculated for both Ga and In peaks, and E is the Ga atomic fraction.

4.2.4 Crystallization Studies

In situ glancing incidence X-ray diffraction (GIXRD) was performed to monitor the onset of crystallization in IGO films. Films were heated in air at 2 °C/min with an Anton Paar heating stage fitted with a graphite dome. The 5.5 minutes Q-range scans from 1.8 to 2.8 $Å^{-1}$ were taken continuously during the annealing processes with a Rigaku Smartlab instrument employing a

multilayer monochromated Cu rotating anode source and point detector. The incident angle of the 8.04 keV X-ray beam was set at 0.6°. The critical angle for In_2O_3 is 0.37° at this energy. The onset of crystallization was determined by the emergence of a crystalline diffraction peak appearing above the amorphous scattering hump. To track the evolution of crystalline fraction (P_{cryst}), a MATLAB script was used to integrate the area under the crystalline diffraction peaks (I_c) and the area under the background-subtracted, total scattering pattern (I_{total}).

$$P_{cryst} = \frac{I_c}{I_{total}}$$

The crystallization temperature is defined as the point at which each film reaches 60% crystallization. To gain more detailed insight into the crystallization kinetics, a more rigorous study would be required and a 2D detector would be needed to quickly sample a larger Q-range.

4.2.5 Structural Characterization

XRR was performed using the Rigaku Smartlab instrument described above. Film data were fit using the Motofit package.[42] XRR fits revealed the overall thickness, electron density, and interfacial thickness for each film. Ellipsometry (J.A. Woollam M2000U Ellipsometer) confirmed the XRR determined thicknesses and provided a measurement of film thicknesses for films beyond the resolution of the multilayer. GIXRD was performed on each film to establish the amorphous nature of the films.

X-ray absorption spectroscopy was performed at the bending magnet 5-BM-D beamline of the DuPont-Northwestern-Dow Collaborative Access Team at the Advanced Photon Source of Argonne National Laboratory. A Si(111) double-crystal monochromator was used to select the

incident X-ray energy. XAS data were collected in fluorescence mode at the In and Ga K-edges, respectively, using a four-element Si-drift detector (Vortex-ME4) with DXP-XMAP electronics (XIA LLC). The films were held vertically with the X-ray incident angle at 54°. The emitted fluorescence signals were collected with the detector at 90° to the incident X-ray beam. The deadtime effect was carefully monitored, and the total X-ray intensities measured by the detector were kept low so that this effect is negligibly small in the measured XAS spectra, typically, smaller than the error due to the data statistics and much smaller than the error bars for the coordination number. Data analysis and extended X-ray absorption fine structure (EXAFS) fitting were performed with the iXAFS package.[43] Fittings of the first shell structure were performed in real space in the R-range of 1.0–2.15 and 1.0-2.36 Å for the Ga and In K-edges, respectively. The amplitude scaling factors, S_0^2, of 0.98 for the Ga K-edge and 1.04 for the In K-edge were determined from fits of the two crystalline reference samples (In_2O_3 and Ga_2O_3).

4.3 Results and Discussion

4.3.1 Transistor Fabrication and Characterization

Control of temperature and O_2 partial pressure is important for producing high-performing PLD films. PLD channel layers were grown at 25 °C in 48.5 mTorr of O_2. A temperature of 25 °C ensures that films are fully amorphous and have the highest possible mobility.[28] It is also necessary to optimize the O_2 partial pressure; reducing it in the deposition chamber by only 3 mTorr results in films that are conductive, having too many free carriers to create functional TFTs. Note that the importance of the O_2 environment has also been reported in sputtered a-IGO films.[39,44] PLD devices with channel layers containing 9.3 atomic precent (at. %) Ga (IGO9.3) exhibit the highest

saturation mobility (μ_{sat}), 42.13 cm^2 V^{-1} s^{-1} (Table 4.1). PLD-derived IGO transistors have not been previously reported. However, excellent-performing sputtered a-IGO channel layers having mobilities between 27 and 43 cm^2 V^{-1} s^{-1} have been reported,[39,44] in good agreement with the present results.

Table 4.1. Performance Metrics of Top-Contact/Bottom-Gate TFTs Fabricated with 10-15 nm a-IGO Channel Layers Films Grown on SiO_2/Si with Al contacts, Fabricated via PLD, Spin-CS, or Spray-CS[a]. ([a] From ≥ 10 devices made on each representative film.)

Composition	μ (cm^2 V^{-1} s^{-1})	V_{th} (V)	V_{on} (V)	Log (On/Off)	SS (V/dec)
PLD IGO 9.3	42.13 ± 0.87	9.65±0.94	-1.80 ± 0.63	6.76 ± 0.11	1.27 ± 0.07
PLD IGO 18.0	20.05 ± 5.31	-67.40 ± 10.43	-74.80 ± 2.39	3.65 ± 0.97	8.02 ± 4.91
PLD IGO 28.0	16.21 ± 4.32	-24.30 ± 6.51	-28.70 ± 1.95	5.89 ± 0.40	1.84 ± 0.34
PLD IGO 35.0	4.56 ± 2.06	-1.09 ± 8.92	-8.20 ± 1.32	6.16 ± 0.41	1.20 ± 0.14
PLD IGO 9.3	25.81 ± 10.98	-15.82 ± 10.97	-21.05 ± 3.63	6.22 ± 0.59	1.79 ± 0.46
PLD IGO 18.0	15.46 ± 6.96	-47.88 ± 99.70	-73.86 ± 4.14	3.78 ± 1.53	5.14 ± 2.13
PLD IGO 28.0	10.98 ± 1.01	-21.55 ± 1.71	-32.90 ± 1.52	4.84 ± 0.43	2.76 ± 0.48
PLD IGO 35.0	4.74 ± 1.85	-2.49 ± 9.01	-6.20 ± 1.03	5.92 ± 0.16	1.32 ± 0.09
Spin IGO 13.9	17.67 ± 1.15	-13.96 ± 11.35	-25.78 ± 4.76	4.95 ± 1.13	4.30 ± 5.07
Spin IGO 25.6	10.60 ± 0.22	4.85 ± 2.31	-13.22 ± 7.33	6.20 ± 0.41	2.11 ± 0.98
Spin IGO 39.1	9.52 ± 1.05	6.21 ± 6.59	-7.88 ± 3.80	6.64 ± 0.22	1.69 ± 0.55
Spin IGO 50.9	2.51 ± 0.54	10.13 ± 2.08	-0.22 ± 1.20	6.67 ± 0.26	1.44 ± 0.20
Spin IGO 13.9	13.42 ± 1.03	-34.60 ± 11.50	-36.63 ± 0.52	2.36 ± 0.50	18.18 ± 7.34
Spin IGO 25.6	8.35 ± 1.56	-4.27 ± 5.47	-14.50 ± 5.76	6.22 ± 0.34	1.80 ± 0.20
Spin IGO 39.8	6.67 ± 0.49	11.85 ± 2.04	-7.00 ± 2.35	6.84 ± 0.06	1.92 ± 0.24
Spin IGO 49.2	2.96 ± 0.42	21.17 ± 2.35	3.80 ± 4.15	6.27 ± 0.04	2.53 ± 0.30
Spray IGO 18.2	5.52 ± 0.49	4.92 ± 5.23	-12.00 ± 4.67	5.19 ± 0.17	2.88 ± 0.34
Spray IGO 26.2	6.60 ± 0.16	9.67 ± 2.04	-8.50 ± 2.46	5.64 ± 0.30	2.13 ± 0.31
Spray IGO 33.1	6.74 ± 0.35	9.03 ± 1.55	-6.70 ± 1.64	5.70 ± 0.23	1.99 ± 0.21
Spray IGO 42.3	5.03 ± 0.23	12.98 ± 0.82	-2.00 ± 1.25	6.02 ± 0.29	1.68 ± 0.24
Spray IGO 18.2	4.51 ± 0.64	9.70 ± 4.60	-8.30 ± 3.02	5.34 ± 0.27	2.47 ± 0.32
Spray IGO 26.2	19.99 ± 1.37	-12.68 ± 5.17	-31.00 ± 3.00	5.00 ± 0.58	3.48 ± 0.99
Spray IGO 33.1	5.85 ± 0.83	10.17 ± 5.62	-4.60 ± 5.60	6.23 ± 0.43	1.58 ± 0.30
Spray IGO 42.3	2.72 ± 0.71	-0.33 ± 7.71	-6.40 ± 8.83	5.74 ± 0.54	2.03 ± 1.01

Direct control of O_2 content is not possible during CS growth because film deposition takes place in ambient air and not within a vacuum chamber. However, a previous study which varied the Ga content in IGZO Spin-CS films suggested, via X-ray photoelectron spectroscopy (XPS) results, that Ga is an oxygen "getter" and increases metal-oxygen-metal bonding. Spin-CS channel layers were fabricated at 300°C. This temperature represents an optimization between improving film performance and enabling the option of depositing on low-cost flexible plastic substrates.[32] The highest μ_{sat}, 17.67 $cm^2 V^{-1} s^{-1}$, was measured on the film with the lowest Ga content, mirroring the trend in PLD devices (Table 4.1). The μ_{sat} values of the IGO13.9 devices represent a significant increase over other traditionally solution-processed via sol-gel IGO TFTs with reported mobilities ranging between 1.0-12.7 $cm^2 V^{-1} s^{-1}$. Note that the mobility of 12.7 $cm^2 V^{-1} s^{-1}$ is from a film processed at 500 °C and is incompatible with flexible plastic substrates.[15,16,40,41,45–48] The similarity in the downward mobility trend, with increasing Ga content, of PLD and Spin-CS devices represents an opportunity to utilize PVD-based knowledge to understand the Spin-CS performance.

Spray-CS channel layers were initially grown at 250 °C where all films are amorphous across the entire In-Ga composition space. Previous work has shown that crystallinity can significantly influence carrier mobility and that partially crystalline films exhibit the lowest mobility (Figure 4.2).[28] Thus, for a more direct comparison we wanted all films to be amorphous as-deposited. However, charge transport was immeasurably low in Spray-CS films grown at 250 °C so that functioning TFTs were unobtainable. Nevertheless, functioning IGO TFTs can be fabricated with Spray-CS films grown at 300 °C. The device with the highest μ_{sat} for a Spray-CS film was fabricated with an IGO26.2 film. However, the large spread in μ_{sat} values for IGO26.2

film devices results in a standard deviation >2× higher than for devices made with all other Spray-CS films. This discrepancy is likely due to the partially crystalline nature of the IGO26.2 films (Figure 4.2 and Figure 4.3) and highlights the importance of thermal phase stability in amorphous films for creating reproducible devices.

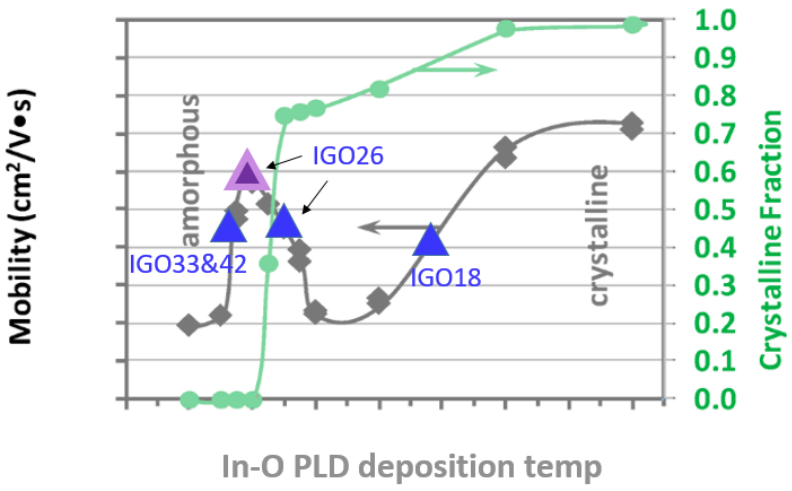

Figure 4.2. Comparison of Film Crystallization Fraction and Mobility. An illustration of how phase instability in Spray-CS IGO (blue triangles) may explain the range of mobility values. Adapted from work on PLD In-O by Buchholz et al.[28]

It is not crystallization but rather the co-existence of both crystalline and amorphous phases which has been shown to degrade mobility in PLD amorphous oxides (Figure 4.2). Therefore, it is important to have films which are fully amorphous. For solution-processed films the processing temperature must strike a balance between being high enough to remove solvent molecules but low enough to avoid melting the substrate or inducing partial crystallinity. We do not expect a correlation between high thermal stability and room temperature mobility measurements. However, thermal phase stability is important for ensuring film performance does not change

during aging or post deposition processing. Spray-CS IGO26 devices display a wide range of mobility vales and the 300°C deposition temperature of the Spray-CS channel layers is very close to the crystallization onset temperature of Spray-CS films with 20-30 at. % Ga. Thus, we propose the structure of Spray-CS films may be inconsistent between preparation of devices on different films, and the inconsistent structure affects the performance of otherwise comparable devices.

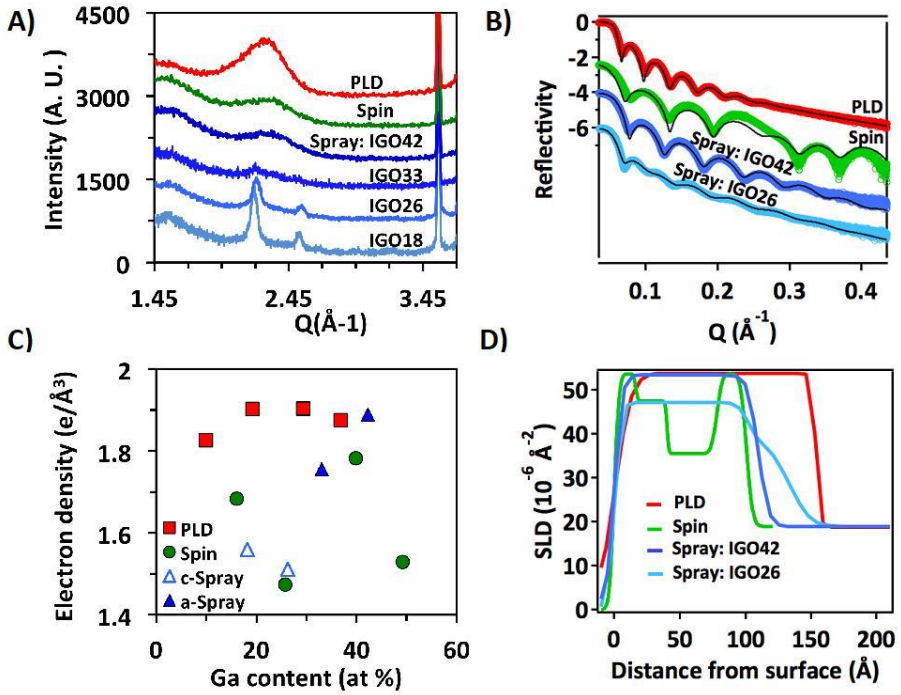

Figure 4.3. X-ray Scattering Data for IGO TFT Films Grown by PLD, Spin-CS, and Spray-CS. The PLD IGO30 films are shown in red, the Spin-CS IGO40 films processed at 300°C are green, and the Spray-CS films are blue with the Ga content indicated. A) GIXRD patterns of as-deposited IGO films before the deposition of Al contacts. Note that at low Ga content, Spray-CS films are partially crystalline and display Bragg reflections at Q values of ~2.2 and 2.5. The (400) reflection from the Si substrate can be seen at Q ~3.6 $Å^{-1}$. B) XRR data (circles) and fits (black lines) of as-deposited IGO films. C) XRR determined electron density of each TFT channel layer. Films with multiple layers are presented as the average density of all layers. Crystalline Spray-CS films (c-Spray) are shown as open triangles while amorphous Spray-CS films (a-Spray) are shown as filled-in triangles. D) XRR determined scattering length density (SLD) as a function of distance from the surface of the film. The Spray-CS IGO26 film is partially crystalline and is fit best with a 2-layer model.

Besides deposition temperature, cation ratios must also be controlled to optimize a-MO channel-layer performance. Here we use the simple two-cation system IGO, where the Ga/In ratio is slowly modified to produce Ga-dependent property trends. The cation ratio is easily measured and controlled in all three film growth processes. Comparing the IGO series, rather than single discrete compositions, enable the effect of processing method on TFT performance to be more effectively evaluated. In addition, it enables previous studies to be leveraged when developing an understanding of Spin- and Spray-CS TFTs.

Ga-dependent mobility was explored for all three growth processes. Both Spin-CS and PLD TFTs exhibit a downward trend in μ_{sat} with increasing Ga content (Figure 4.4A). This trend has previously been reported in both TFT-derived mobility[15,39,47] and Hall mobility[49] for a-IGO films grown by sputtering[39,49] and solution-processing methodologies.[15,47] Recent work, using gated Hall-effect measurements, suggests Ga influences transport in a-oxide semiconductors.[50] More specifically, molecular dynamics simulations combined with density functional theory illustrate that the preference of Ga to remain 4-fold coordinate is effective in disordering and disrupting the conduction manifold and thus decreases mobility.[27,51] Here, we expand this study by providing evidence, through extended X-ray absorption fine structure (EXAFS) analysis (Figure 4.5), that the 4-fold coordinate Ga mechanism is also present in CS films. In addition to disrupting and disordering, 4-fold coordinate Ga is also found to be a significant source of traps.[27] We show that 4-fold coordinate Ga contributes traps in both PLD and Spin-CS TFTs, as indicated by the increase in the hysteresis between the forward-and-reverse voltage sweeps (Figure 4.6) as the Ga substitution level increases. No significant Ga-dependent trends are seen in the present Spray-CS films, suggesting that the Spray-CS processing conditions have the dominant influence

on the μ_{sat} and trap density in this set of films. Along these lines, the subthreshold swing is large, and μ_{sat} is similar for all Spray-CS devices, regardless of IGO composition.

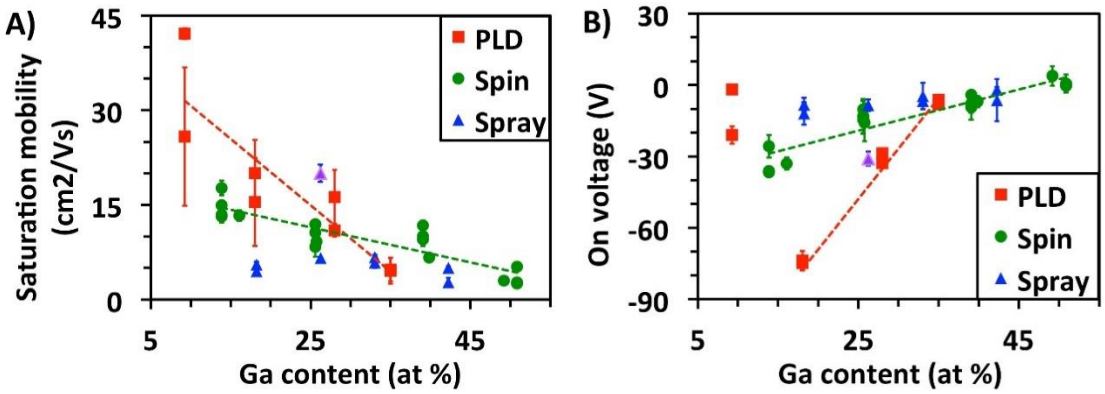

Figure 4.4. Mobility vs. Ga Content and On Voltage vs. Ga Content Plots for IGO TFTs. Saturation mobility A) and on voltage B) of TFT devices made with a-IGO channel layers deposited by PLD (red squares), Spin-CS (green circles), and Spray-CS (blue triangles). Each point represents a separate film deposition. More than 10 devices were measured on each film; error bars represent the standard deviation between devices. Dashed lines represent linear best fits of PLD (red) and Spin-CS (green) data and are provided to highlight Ga-dependent trends. For the Spray-CS IGO26 metrics, the purple triangle represents the average of devices made on an amorphous Spray-CS IGO26 film while the blue triangle is an average of devices on the partially crystalline Spray-CS IGO26 films shown in Figure 4.2.

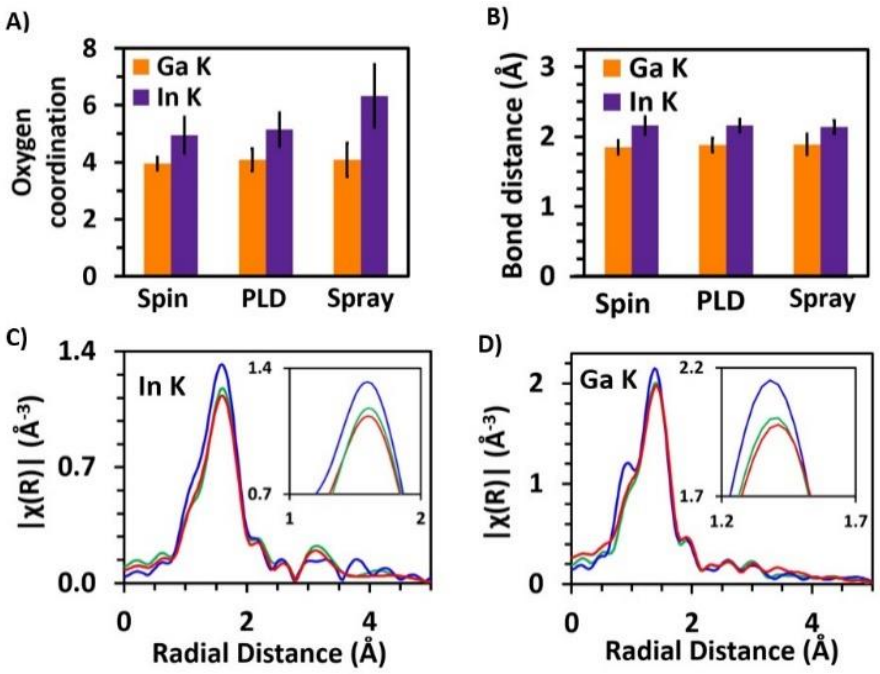

Figure 4.5. Comparisons from the In K-edge and Ga K-edge EXAFS Data for PLD, Spin-CS, and Spray-CS IGO Films. The PLD films were grown at 7.5 mTorr, and the Spray-CS films were grown at 250 °C. A) Comparison of M-O coordination. B) Comparison of M-O bond lengths. C) In K-edge and D) Ga K-edge comparisons of the pseudoradial distribution functions for IGO30 PLD films (red), IGO40 Spin-CS films (green), and IGO33 Spray-CS films (blue).

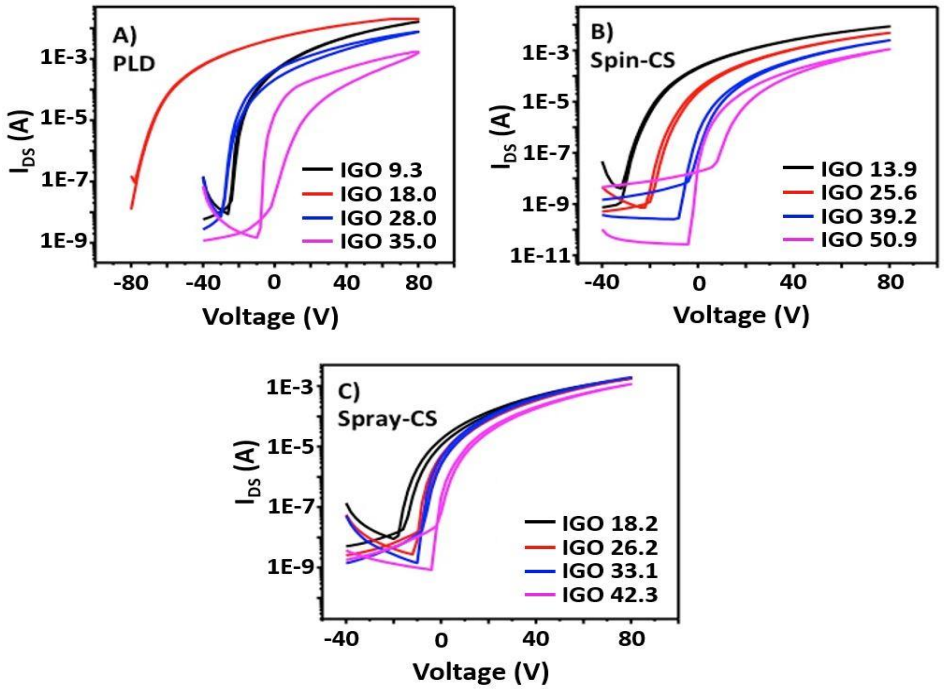

Figure 4.6. Plots of Forward-to-Reverse Voltage Sweeps for IGO TFTs. The a-IGO channel layers were deposited via A) PLD, B) Spin-CS, and C) Spray-CS.

In comparing PLD devices to the solution-processed devices (Spin-CS and Spray-CS), μ_{sat} is clearly the device metric where the PLD films are superior. The consistently high as-deposited film densities (Figure 4.3D) are likely a contributing factor. Low-density a-MO films have been shown to contain voids which decrease electron mobility.[23,52] Similarly, low-density films also have low thermal conductivity, as will be discussed in the next section. It is important to clarify that it is how the metal-oxygen polyhedral building blocks are packed which determines the macroscopic film density, not the metal-oxygen coordination numbers. In this way the very local few-angstrom scale of the film may seem "dense", but the larger nanometer-scale structure of the film can contain voids and thus have a very low density. For instance, the crystalline as-deposited Spray-CS films have high oxygen coordination numbers but very low density. These partially

crystalline films may be thermodynamically locked into a porous structure during deposition and unable to kinetically relax like the amorphous films. In addition to the mixed crystalline-amorphous phase structure (Figure 4.2), the low density of the partially crystalline Spay-CS films may explain why the trend of increasing mobility with decreasing Ga content is not seen here for the Spray-CS devices.

While high mobility is important for fast devices, a near-zero V_{th} is important for efficient TFTs. Ga-dependent V_{th} was explored for all three film growth processes. V_{th} is related to carrier concentration; the fewer the number of carriers, the more applied voltage it takes to turn the device on. Threshold voltage (V_{th}) and on voltage (V_{on}) are very similar. The threshold voltage is defined as the minimum gate-to-source voltage required to form the conduction channel between the source and drain electrodes. V_{th} values are derived from fitting the transfer curve. In comparison, V_{on} is determined by looking for the voltage at which the difference between the off current and on current become significant enough for the device to be defined as on. In turn, V_{on} is less dependent on irregularities in fitting.

As with mobility, a clear trend in carrier concentration versus Ga/In ratio is known and understood for PLD-grown devices.[27] This trend is also seen in this study. An uptrend in a-IGO TFT V_{th} with increasing Ga content is established for all Spin-CS and PLD TFTs having >10 at. % Ga (Figure 4.4B and Table 4.1). The increasing V_{th} suggests that carrier concentrations decrease with increasing Ga content and is in accord with reduced a-IGO carrier concentrations with added Ga reported previously from transistor[15,41,47] and Hall measurements.[49] The mechanism by which Ga modulates carrier concentrations is attributed to the high Ga-O binding affinity.[27] Oxygen vacancy-like defects formed around low-oxygen coordinated In centers are the primary source of

carriers in a-IGO.[27] Previous work suggests that Ga creates an unfavorable environment for forming carrier-producing defects. Thus as Ga is substituted for In, these carrier-producing defects are reduced. A significant range of V_{th} and on voltage (V_{on}) values have been reported for a-IGO TFTs deposited via sputtering (-14 to 3.05 V)[39,44] and solution processing (-17 to 15.1 V).[40,46-48] In Table 4.1, we report values of V_{th} and V_{on} for the current work.

Differences in V_{th} are also seen when comparing devices with channel layers grown by the different methods. PLD devices are found to almost always operate in depletion mode, where V_{th} is negative (Table 4.1). In depletion mode, transistors must be driven while in the off state. Devices fabricated from IGO18 PLD films are especially conductive, with V_{th} falling below -60 V; while surprising, this result is robust and was reproduced multiple times. In contrast, the present Spray-CS and Spin-CS films have higher V_{th} values, with the majority of films having positive V_{th} values. V_{th} for Spray-CS films suggests that all Spray-CS films operate in enhancement mode, where V_{th} is positive. The more positive values of V_{th} for Spray-CS over the Spin-CS and PLD films (Table 4.1) suggest that the Spray-CS processing method is especially effective at reducing the carrier concentrations.[39] The EXAFS analysis in this study (Figure 4.5) reveals the mechanism: Spray-CS films have high In-O coordination numbers, as compared to the other growth methods (Figure 4.5A), indicating that the oxygen vacancy-like defects around the In atoms (the source of carriers) are correspondingly low. The fine mist created during Spray-CS presumably enables rapid solvent evaporation and likely high O_2 exposure of the metal ions, leading to well-formed metal-oxygen polyhedra and low densities of oxygen vacancy-like defects (i.e., carriers).[23] Again it is important to note that it is the packing of metal-oxygen polyhedral building blocks which determines the macroscopic film density and not the metal-oxygen coordination numbers.

Overall, the highest performing PLD transistors identified in this study are those fabricated from IGO9.3 films. These devices have the highest average μ_{sat}, reasonable V_{th}, and no visible hysteresis (Figure 4.6). Note, however, that output plots of the PLD transistors (Figure 4.7) suggest there may be issues with charge injection in some devices and that Al contacts may not be perfectly ohmic for these devices. Better performance may be achieved through contact optimization.[53] Consistent with other a-IGO solution-processing techniques,[15,41] the highest performing Spin-CS films are those grown in the 25-40 at. % Ga composition range. These consistently display above average μ_{sat} values for solution-processed films (6.67-11.92 $cm^2 V^{-1} s^{-1}$), have limited hysteresis, competitive on/off current ratios (10^6 – 10^7), and positive V_{th} values. Although slightly underperforming in comparison to Spin-CS devices, the Spray-CS devices still exhibit very good TFT performance for solution-processed films.[4] The only metric where Spray-CS truly underperforms, in comparison to the other processing methods in this work, is μ_{sat}. The significant difference in density for Spray-CS deposited at 300 °C (Figure 4.3C) versus at 250 °C (Figure 4.11) highlights the strong dependence of Spray-CS film electronic properties on processing parameters. The Spray-CS method is still relatively new. With additional rounds of optimization, Spray-CS films have the potential to perform as well as, or even outperform, Spin-CS derived films.

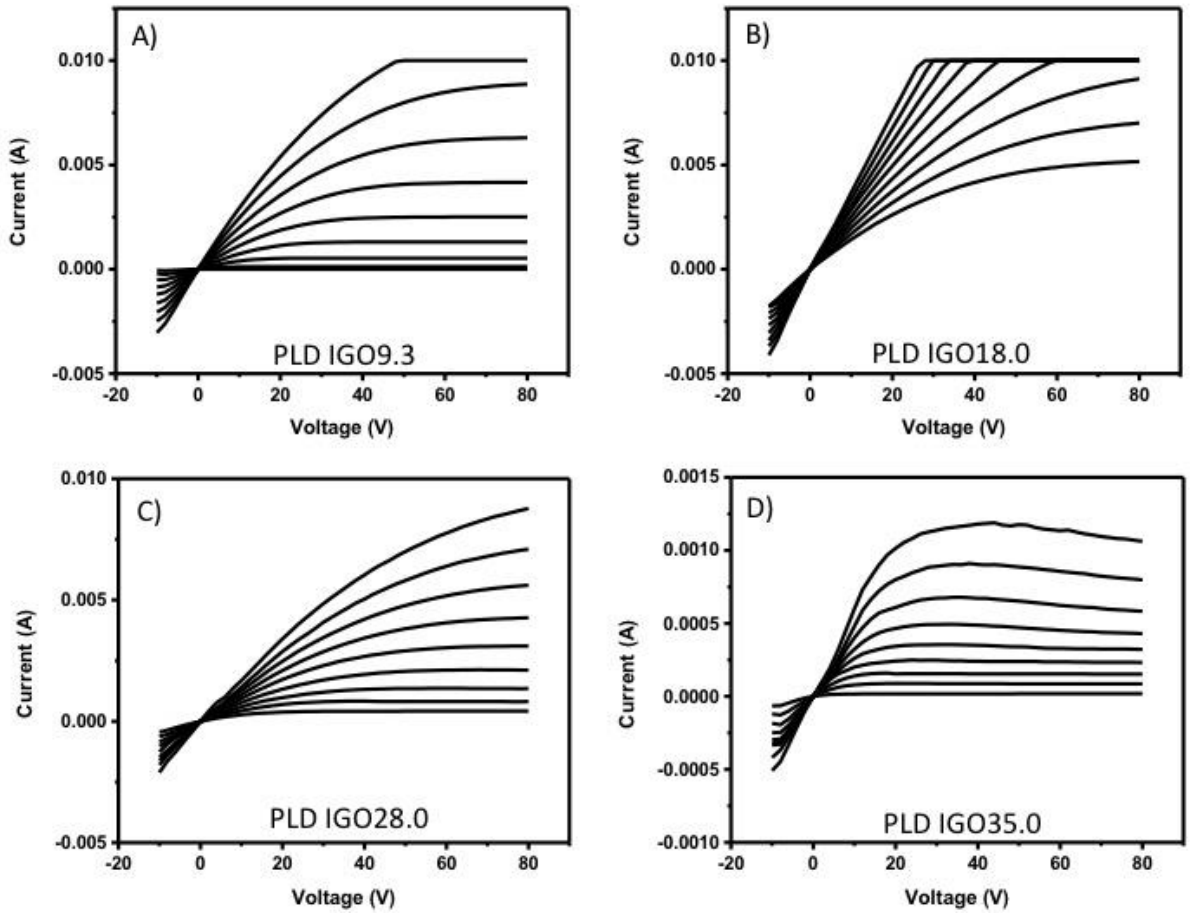

Figure 4.7. PLD Output Plots for IGO TFTs at Different Ga Concentrations. A) 9.3 at. % Ga, B) 18.0 at. % Ga, C) 28.0 at. % Ga, and D) 35.0 at. % Ga.

4.3.2 Thermal Structural Stability

Thermal phase stability is important for maintaining robust device performance throughout multiple thermal processing steps and operation in hot climates. However, post-deposition thermal stability of a-MOs is rarely studied. To understand the interplay of deposition method on thermal phase stability of film structure, *in situ* GIXRD measurements were performed during air annealing studies. Films were heated at a constant rate of 2 °C/min so that crystallization kinetics[29] would be

sufficiently slow to record multiple 5.5 minute diffraction scans during the crystallization process. Series of a-IGO film compositions deposited by PLD, Spray-CS, or Spin-CS were studied. From the GIXRD data the crystalline phase fraction can be tracked over time and temperature (Figure 4.8). The onset of crystallization (T_{onset}) and crystallization temperature (defined as the temperature at which 60% crystallization is achieved) are plotted as a function of Ga content and deposition method (Figure 4.9).

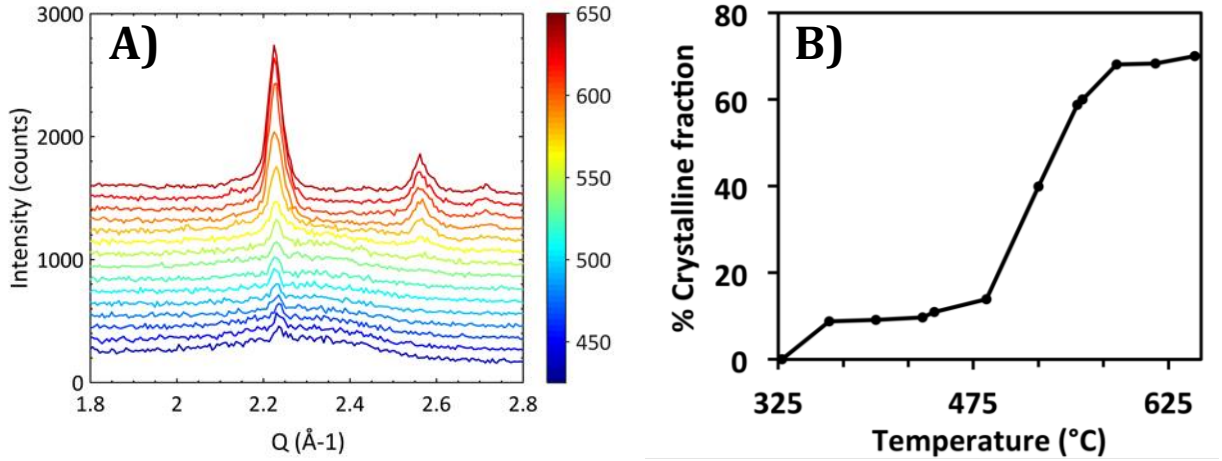

Figure 4.8. Continuous Air Annealing GIXRD Patterns and Percent Crystalline Fraction vs. Temperature Plot of a Spin-CS IGO Film. A) GIXRD patterns are taken continuously during air annealing. Films are heated inside a graphite dome at a rate of 2 °C per minute. 2θ scans each lasted 5.5 minutes. B) Percent crystalline fraction of Spin-CS IGO17 sample plotted as a function of median scan temperature.

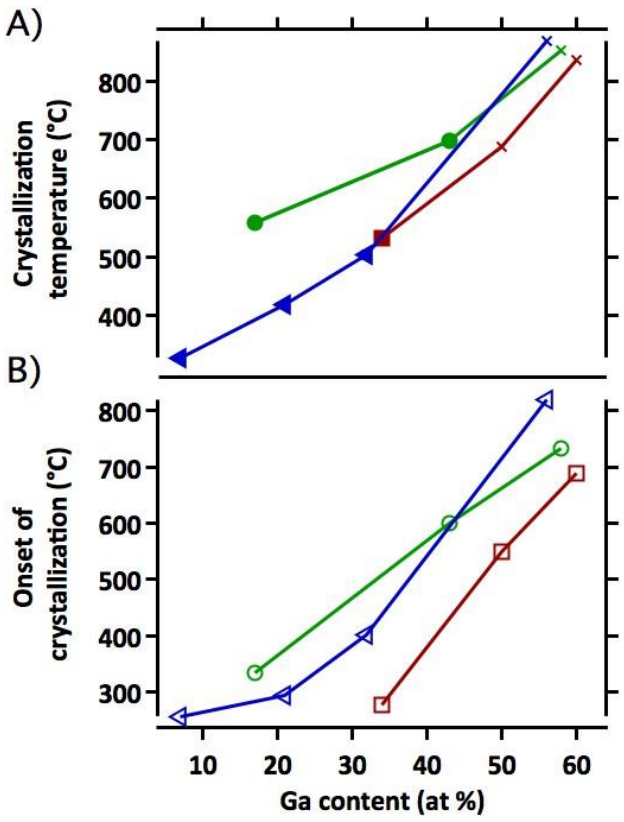

Figure 4.9. Crystallization Temperature Data vs. Ga Content Plots for IGO Films. A) Crystallization temperature and B) temperature at the onset of crystallization, of Spin-CS (green), Spray-CS deposited at 250 °C (blue), and PLD (red) a-IGO films as a function of at. % Ga. Data points indicated by × in A) represent those which required extrapolation due to sample deterioration or instrumental temperature limitations.

As with TFT performance, Ga-dependent trends in thermal phase stability are observed. A Ga-dependent trend was previously demonstrated in an *ex situ* study of PLD IGO,[27] the crystallization temperature rose with the addition of the substitutional Ga cation. This trend is seen for all processing methods, even Spray-CS which did not show Ga-dependent TFT performance. Leveraging previous PLD studies,[27,54,55] we can understand the mechanism: Ga prefers to remain

~4-fold coordinate, in contrast to the surrounding In-O matrix, thus inhibiting the onset of crystallization. The EXAFS analysis of oxygen coordination (Figure 4.5 and Figure 4.10) establishes the persistence of ~4-fold coordinate Ga for all compositions and all processing methods (Figure 4.5). The short Ga-O bond distances provide additional support for the low Ga-O coordination numbers (Figure 4.5). From Figure 4.9, it is clear the Ga concentration is the dominant factor in determining thermal phase stability of a-IGO films.

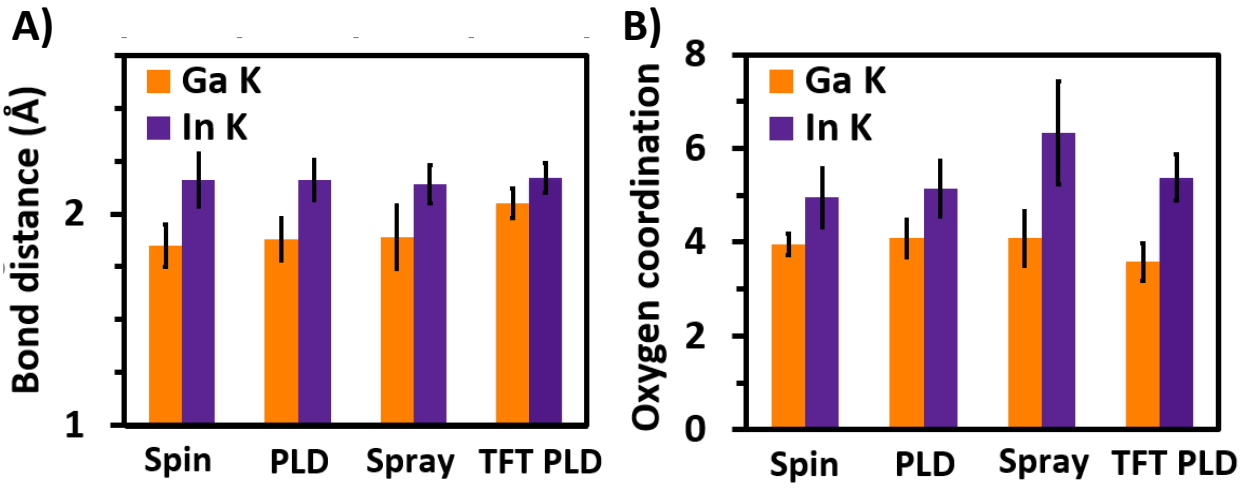

Figure 4.10. Bond Distance and First-Nearest Neighbor Coordination for IGO Films. A) Bond distance comparison and B) first-nearest neighbor coordination comparison for average Spin-CS films, Spray-CS films, and PLD (7.5 mTorr) and PLD TFT (higher oxygen during deposition to make good transistors).

The PLD films exhibit the lowest thermal structural stability. The onset of crystallization occurs at lower temperatures than either the Spin- or Spray-CS films; this trend holds true for all a-IGO compositions. A likely reason is that heat is not dissipated in burning off organic residue as in the CS films. XPS studies of both Spin- and Spray-CS films reveal residual organic material in

the as-deposited films.[24,40] In contrast, PLD takes place in a vacuum and thus does not have residual organics. XRR scans taken before and after annealing show (Figure 4.11) the as-deposited PLD films have relatively high densities. Recent work by Cui et al.[56] on a-IGZO determined that thermal conductivity decreases linearly with film density. Therefore, the denser PLD films may crystallize more rapidly because they have the highest thermal conductivity. XRR results also reveal that the present as-deposited PLD films are closest in density to their final crystalline density (Figure 4.11C). Therefore, the structural rearrangement required for PLD films to crystallize may be reduced versus the Spin- and Spray-CS films.

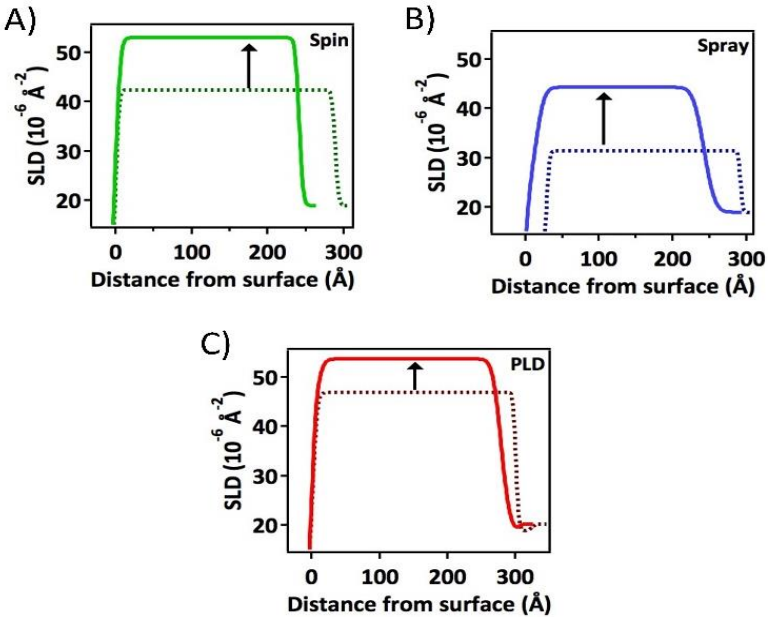

Figure 4.11. Scattering Length Density Before and After Crystallization for IGO Films. Scattering length density showing the increase in density and decrease in thickness from before crystallization (dotted line) to after crystallization (solid line) for a representative Spin-CS (green, A), Spray-CS deposited at 250 °C (blue, B), and PLD (red, C) film.

The Spin-CS films exhibit the highest thermal phase stability below ~45 at. % Ga and 600 °C. The XRR data of Spin-CS films highlight their layered nature (Figure 4.3D) that results from the layer-by-layer spin-coating process (Figure 4.1C). The presence of distinct layers in Spin-CS films has been noted previously.[57–59] These layers likely play a role in the crystallization mechanism and may hinder the structural relaxation that takes place upon crystallization.[38] Additionally, the film may act as multiple very thin films, as opposed to a thick film. Very thin films (~25 Å) are known to have slower crystallization rates due to their higher interface-to-bulk ratio.[60,61] Care was taken to ensure that the bulk thickness of all as-deposited films in the crystallization study were equivalent.

For the thermal phase stability studies, all Spray-CS films were grown at 250 °C to ensure that these as-deposited films were amorphous. The onset of crystallization is found to occur below 300 °C for films with Ga contents below 22 at. % Ga (Figure 4.9), providing insight into why Spray-CS films deposited for TFTs at 300 °C are crystalline in the low Ga regime. Low Ga content Spray-CS films initially have lower thermal phase stability than Spin-CS films. However, they outperform both Spin-CS and PLD films in the high-Ga, high-temperature growth regime. Note that unlike the more linear trend in T_{onset} versus Ga content seen in PLD and Spin-CS films, the thermal phase stability of Spray-CS films becomes increasingly dependent on Ga content at high Ga substitution levels. Interestingly, the density of the crystallized Spray-CS films deposited at 250 °C is lower than that of both crystallized PLD and crystallized Spin-CS films (Figure 4.11). Previous studies on the IGO system have shown that In-O coordination number rises during crystallization;[27] this coordination number increase is due to either structural relaxation[28,35,38] (i.e., densification), O_2 uptake into the film, or, more likely, a combination of both mechanisms.[62]

Because high In-O coordination numbers (Figure 4.5) are already achieved in as-deposited Spray-CS films, the level of densification required for crystallization may be lessened. We also note that the as-deposited density of the amorphous Spray-CS films grown at 250 °C is very low, which may explain why these films have low electrical performance and why their density after crystallization is still low when compared to PLD and Spin-CS films.

4.4 Conclusions

PLD, Spin-CS, and Spray-CS film processing methods are compared in the a-IGO system across a broad range of Ga substitution levels. The thermal phase stability of amorphous oxide films is found to be significantly influenced by the processing method and Ga substitution level. Films grown by combustion processing methods have higher thermal phase stability than films grown by PLD. For all processing methods, the a-IGO thermal phase stability can be tuned by controlling the film Ga content.

The results of PLD and Spin-CS TFTs suggest that these processing methods are responsive to composition-dependent property tuning. Increasing the Ga content is shown to decrease μ_{sat}. The mechanism is understood by EXAFS analysis to be caused by the introduction of Ga-O polyhedra, which have a distinctly different structure from the surrounding In-O matrix; this distinct structure disrupts carrier mobility and produces traps. PLD films are revealed to have the highest carrier mobilities due in part to their superior density.[23,52,63] Increasing the Ga content is also shown to increase V_{th} for Spin-CS and PLD devices. The mechanism is understood to be the result of a decrease in free carriers. The 4-fold oxygen-coordinated Ga, seen with EXAFS analysis, does not produce carriers. Instead, carriers form around undercoordinated In centers.[27]

EXAFS analysis illustrates that Spray-CS films contain high In-O coordination, which results in a lack of carrier producing defects and explains the consistently near-zero V_{th} values of Spray-CS devices.

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