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Modeling, Imaging, and Processing for Printed van der Waals Thin-Film Optoelectronics

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Abstract

Modeling, Imaging, and Processing for Printed van der Waals Thin-Film Optoelectronics

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This thesis explores the potential of two-dimensional (2D) or van der Waals (vdW) materials for printed optoelectronic devices. The research focuses on the development of processing, imaging, and modeling of materials and thin-film devices to optimize performance and introduce novel properties.

A gate-dependent resistor network model is presented that establishes distinct microstructure-performance relationships arising from near-edge and intersheet resistances in printed thin-film transistors. The model predicts that the removal of edge states can lead to higher mobilities, motivating the research in developing edge functionalization strategies. The study also examines the origin of the photoresponse in printed photodetectors. Optical microscopy-based methods were employed to determine the device topography, while local photoimpedance spectroscopy was used to characterize the photoconductive behavior. Lastly, the thesis investigates device concepts based on variable ion-binding rates in photoswitchable molecules and suggests future directions for developing hybrid organic-inorganic materials that facilitate the integration of memory with logic.

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Chapter 1   Introduction

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1.1.   Thin-Film Transistor Applications, Design Targets, and Materials

The development of thin-film transistors (TFTs) on large-area substrates at low cost has enabled flexible displays,[2] sensors,[3–5] microprocessors,[6] and electronic tags[7] for emerging microelectronics, wearables, and the Internet of Things.[8] To optimize drive current and switching frequency while minimizing power consumption in TFTs, it is crucial to maximize the effective mobility of the semiconducting channel material while maintaining a high on/off ratio; high-end display applications typically demand transistors with an effective mobility of 10 $cm^2V^{-1}s^{-1}$ and an on/off ratio of 10^6 (refs.[9,10]).

The mobility and on/off ratio are strongly influenced by the microstructure and geometry of the channel. Consequently, materials and device engineers face the challenge of designing processes that optimize microstructure while considering constraints on cost, complexity, deposition method, and processing temperatures. For instance, polycrystalline silicon can exhibit mobilities of 50-100 $cm^2V^{-1}s^{-1}$(ref. [11]), but the required processing temperatures (>500 °C) inhibit integration with plastic substrates. In contrast, amorphous silicon thin films can be deposited over large areas at temperatures below 100 °C, but the effective mobility of 0.5-1 $cm^2V^{-1}s^{-1}$ limits their use to applications such as low-end liquid-crystal displays and electronic paper.[10] Amorphous indium gallium zinc oxide (IGZO) can reach a mobility of 10 $cm^2V^{-1}s^{-1}$ (ref. [12]) when deposited

from the vapor phase at room temperature, but the lack of p-type metal oxides with performance comparable to IGZO limits its application in complementary logic devices[10] and the pulsed laser deposition process is expensive compared to other methods.[13]

Recently, two-dimensional (2D) or van der Waals (vdW) materials have emerged as promising candidates for large-area flexible electronics.[9] With properties ranging from insulating to semiconducting to metallic, key device components can be fabricated by assembling various 2D materials into heterostructures.[14] Furthermore, solution dispersions of 2D materials (*i.e.*, 2D material inks) allow large-scale, maskless print-in-place fabrication of thin-film electronics on plastic substrates,[15–19] reducing process complexity and manufacturing cost. However, the relationship between the microstructure of printed 2D thin films and their performance in TFTs remains poorly understood, impeding the optimization of fabrication processes, including exfoliation, ink formulation, and deposition.

1.2. Status Quo of Printed vdW TFTs and Limiting Factors

A wide range of effective mobilities (0.001-10 $cm^2V^{-1}s^{-1}$) has been reported for printed vdW TFTs.[15,16,20–29] The mobility is influenced by both the thin film microstructure, *i.e.,* how individual sheets are connected, and the mobility of individual sheets, which is sensitive to defects created during the exfoliation process. Focusing on MoS_2 as a representative channel material, which typically exhibits a field-effect mobility of ~100 $cm^2V^{-1}s^{-1}$ at room temperature in single crystal form, the highest performing printed devices to-date were fabricated by spin-coating electrochemically exfoliated few-layer MoS_2 nanosheets.[26] These films demonstrated significant basal plane overlap between adjacent flakes and effective channel mobilities of 7-11 $cm^2V^{-1}s^{-1}$,

which are comparable to single-crystal nanosheets (10 $cm^2V^{-1}s^{-1}$) subject to the same chemical treatment. Hence, it is possible for the mobility of devices with printed channels to approach the single-sheet limit.

However, most printed MoS_2 devices exhibit much lower mobilities. An effective mobility of 0.73 $cm^2V^{-1}s^{-1}$ (ref.[27]) was observed in thin films assembled from electrochemically exfoliated monolayer MoS_2 sheets connected via nanosheet edges instead of overlapping. Low mobilities (~0.1 $cm^2V^{-1}s^{-1}$) were also observed in inkjet-printed TFTs with non-planar stacking of liquid-exfoliated nanosheets (ref.[16]), despite the fact that individual nanosheets isolated from the inks exhibited mobilities of 40-100 $cm^2V^{-1}s^{-1}$. Since solution-based exfoliation processes can yield single-sheet mobilities comparable to tape-assisted mechanical exfoliation, it is crucial to understand when printed 2D transistor performance is limited by junction resistance between nanosheets rather than nanosheet mobility.[30]

As noted above, the best-performing printed devices have adjacent sheets with stacked basal planes, justifying a deeper study of this morphology to understand the origins of junction resistance and the limits placed on mobility. When sheets overlap, junction resistance is determined by two distinct factors: the intersheet resistance (*i.e.*, the resistance between overlapping basal planes) and the near-edge resistance (*i.e.*, the resistance generated by nanosheet edges). Previous studies of vdW TFTs have claimed that the intersheet resistance limits the channel mobility,[16,28,30] which is plausible since solvents and/or binders used in solution processing may introduce contaminants that increase intersheet resistance.[31,32] Mitigation strategies include formulating inks with low boiling-point solvents[33] to reduce contamination and introducing interfacial layers that generate delocalized sp^2 electronic states at the interface[28,34] to promote intersheet charge transfer. Because

$\pi-\pi$ stacking in overlap regions should facilitate intersheet charge transfer,[35] functionalizing with molecules that covalently bond to sulfur vacancies can increase the effective mobility of a printed MoS_2 film.[28]

Near-edge resistance, which has been largely overlooked, can also impair mobility. Nanosheet edges contain a higher density of point defects than the basal plane,[28,36] causing scattering and trapping of charge carriers and reducing mobility.[37] The charge carrier depletion induced by the edge-trapped charges also impacts the intersheet resistance. While the number of trapped charges at nanosheet edges increases monotonically with nanosheet thickness, charge screening varies in a non-linear and complex manner strongly due to the transition from 2D to 3D screening as thickness is increased.[38] Given that both intersheet resistance and near-edge resistance may impact the effective mobility in composite 2D thin films, it is imperative to understand the relationships between film microstructure and effective mobility in order to co-optimize the processes of exfoliation and printing.

1.3. Thesis Outline

In Chapter 2, we discuss the central methodology employed in this work, including modeling, imaging, and processing materials and devices. We outline the development of a resistor network model for simulating two-nanosheet model transistors and printed vdW TFTs, the Y-function analysis for analyzing transfer curves of transistors, *operando* Kelvin probe force microscopy for measuring surface potential of devices under bias, and impedance spectroscopy for investigating the origins of the photoresponse in printed photodetectors. Furthermore, we describe the use of

atomic layer deposition for growing interlayers and various fabrication processes for creating the devices discussed in this thesis.

In Chapter 3, we present a gate-dependent resistor network model that establishes distinct microstructure-performance relationships arising from near-edge and intersheet resistances in printed van der Waals thin-film transistors. The model was calibrated by analyzing the electrical output and surface potential characteristics of model transistors, which consisted of overlapping 2D nanosheets with varying thicknesses that were mechanically exfoliated and transferred. Kelvin probe force microscopy analysis on the model transistors led to the discovery that the nanosheet edges, not the intersheet resistance, limit transport due to their impact on charge carrier depletion and scattering. Our model suggests that when transport in a 2D material network is limited by near-edge resistance, the optimal nanosheet thickness is determined by a trade-off between charged impurity screening and gate screening. We predict that removing edge states can realize higher mobilities with thinner nanosheets, owing to reduced junction resistances and decreased gate screening.

Understanding the operating mechanisms of thin-film devices and their dependency on processing conditions is crucial for optimizing device performance. In Chapter 4, we discuss the origin of photoresponse in printed MoS_2 photodetectors. Utilizing optical microscopy-based methods, we determined the device topography and revealed that the photoresponse primarily arises from the MoS_2 channel. We also found that the inhomogeneous photoresponse within the channel is due to thickness variations that are likely caused by the photonic annealing. By employing local photoimpedance spectroscopy, we confirmed the photoconductive behavior of the

device and established the formation of an ohmic junction between the graphene contacts and the MoS$_2$ channel, which contributes to enhanced photoresponsivity.

Chapter 5 builds upon the findings in Chapter 3 and presents preliminary results and future directions for the development of edge functionalization strategies for printed MoS$_2$ TFTs, as well as outlines principles and approaches for creating interlayers capable of physically and electronically bridging nanosheets to enhance percolation in printed thin films. We find that ALD SnS$_2$ enhances on-state conductivity and field-effect mobility in printed MoS$_2$ channels with low nanosheet density but reduces performance for sufficiently percolative channels. These observations highlight the benefits of passivating edge states, exfoliating thin nanosheets, and printing thin, percolative films.

Incorporating non-volatile memory into TFTs offers a promising avenue for expanding the capabilities of emerging printed circuit technologies. In Chapter 6, we review the literature on photoswitch-modulated devices and conducted preliminary experiments to explore the potential use of the photoswitchable ion-binding property of spiropyran for integrating memory into electrochemical and electrolyte-gated transistors. We determine that the slow switching is likely caused by steric hindrance, which obstructs conformational changes in the solid state. Based on our literature and experimental findings, we propose future directions for developing novel composites capable of achieving both large current modulation and rapid switching simultaneously.

Chapter 2   Methods

Sections 2.1, 2.2, and 2.6.1, and parts of section 2.3 have been published in ACS Nano in 2023 by Zhehao Zhu, Joon-Seok Kim, Michael J. Moody, and Lincoln J. Lauhon, and reprinted with permission from American Chemical Society.[1]

2.1.   Resistor Network Model for Two-Nanosheet Model Systems and Printed Films

In Chapter 3, a gate-dependent resistor network model was developed to validate our interpretation of the KPFM data on MoS_2/MoS_2 model transistors and predict the optimal microstructure for printed thin-film transistors (TFTs). Example notebooks for simulating the model transistors and printed TFTs can be found: Model Printed vdW TFTs.

2.1.1.   Brief Description of the Model

The proposed model (Figure 2.1 and Figure 3.5a) was developed based on a transmission line model for partially overlapping channels,[39] incorporating spatially varying resistivities that are influenced by gate screening[40] and trapped charges at the edges of sheets.[28,36,41] The model includes horizontal resistors that represent the ohmic conduction associated with intrasheet (in-plane) band-like transport in accumulation,[37] which is found to dominate the overall charge transport in printed MoS_2 network at high gate voltages.[42] In addition, vertical resistors are introduced to represent the effective resistance that considers the anisotropic out-of-plane resistivity and the mobile carrier concentration, which depends on the applied gate voltage. The model accounts for gate screening by employing the Thomas-Fermi charge screening theory to estimate the carrier concentration in each monolayer as a function of distance from the dielectric interface (Section 2.1.2).[40] To reduce the number of independent variables, the junction resistance is treated as a function of two

dimensionless independent variables, the near-edge sheet resistance ratio $R_{S,E}/R_S$ and the intersheet resistivity ratio $\rho_{i,E}/\rho_i$. Conditions where $R_{S,E}/R_S > 1$ and/or $\rho_{i,E}/\rho_i > 1$ indicate that the near-edge resistivities are greater than those in the middle of the homojunction, which can be attributed to unscreened charged impurities identified in KPFM analysis (Chapter 3 Section 3.2). Finally, the effective edge lengths, *i.e.*, the size of the regions depleted by trapped charges, are estimated for each thickness by analyzing the 2D and 3D Debye lengths (Section 2.1.3 Figure 2.2).[38]

2.1.2. Calculating the Intrasheet and Intersheet Resistances

The top nanosheet containing k number of monolayers and the bottom nanosheet containing j number of monolayers form an interface as shown in Figure 2.1a. The equivalent resistor network model of the homojunction is shown in Figure 2.1b.
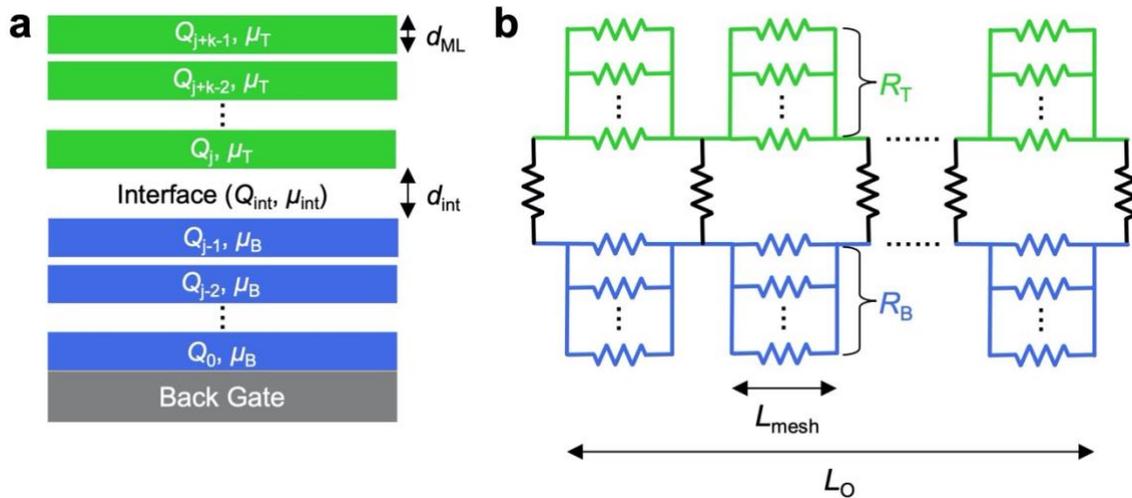
Figure 2.1. (a) Schematic and (b) resistor network model of the two-nanosheet homojunction. Q_i **is the 2D carrier concentration of the ith monolayer counted from the bottom gate.** μ_B **and** μ_T **are the bottom and top in-plane mobilities, respectively.** R_B **and** R_T **are the bottom and top sheet resistances, respectively.** Q_{int}, μ_{int}, **and** d_{int} **are the intersheet carrier concentration, mobility, and distance.** L_{mesh} **is the mesh length.** L_O **is the length of the overlap.**

To calculate the intrasheet resistance of a nanosheet, we first calculate the carrier concentration in each monolayer. By assuming that the gate charges are completely screened by the junction, the 2D carrier concentration of the ith monolayer counted from the bottom gate (*i.e.*, i = 0 to j-1 for the bottom sheet and i = j to j+k-1 for the top sheet) was calculated based on Thomas-Fermi charge screening theory:[40]

$$Q_i \; = \; C_{ox} V_{OV} \left(\frac{1-s}{1-s^{j+k}} \right) s^i \text{ with } s \; = \; \exp(\frac{-d_{ML}}{\lambda_{OP}})$$

(2.1)

where C_{ox} is the dielectric capacitance, d_{ML} is the monolayer thickness, V_{OV} is the overdrive voltage (Equation 2.2), and λ_{OP} is the out-of-plane Debye length (Equation 2.3). The overdrive voltage (V_{OV}) is defined as the difference between the applied gate-source voltage (V_{GS}) and the threshold voltage (V_{TH}) of a transistor (*i.e.*, $V_{OV} \equiv V_{GS} - V_{TH}$).

To simulate the surface potential profiles of the fabricated homojunctions (Figure 3.3, Figure 3.4, and Figure 3.5), the V_{OV} was determined self-consistently at the applied biases where surface potentials were measured:

$$V_{OV} \; = \; \frac{1}{2C_{ox}} (\frac{G_B}{\mu_B} \; + \; \frac{G_T}{\mu_T})$$

(2.2)

where $G_B = (I_{DS}/W)/(dCPD/dx)$ and G_T are the bottom and top sheet conductances, respectively, extracted from linear fits of the measured surface potential profiles in the unoverlapped, single-sheet regions,[43] and μ_B and μ_T are the bottom and top in-plane mobilities, respectively, extracted from transfer curves (Section 2.2). The μ_B, μ_T, and V_{OV} for 8L/8L, 5L/1L, and 1L/1L are given in Table 3.3.

The out-of-plane gate screening was assumed to be 3D with a Debye length:

$$\lambda_{\mathrm{OP}} = \sqrt{\frac{\varepsilon_{\mathrm{OP}} k_{\mathrm{B}} T}{q^2 N_{\mathrm{3D}}}}$$

$$\text{(2.3)}$$

where $\varepsilon_{\mathrm{OP}}$ is the out-of-plane permittivity at the junction and $N_{\mathrm{3D}} = 10^{18}$ cm^{-3} is the typical dopant concentration for our mechanically exfoliated MoS$_2$. The material constants used in the simulations are summarized in Table 2.1.

After calculating the carrier concentrations, the 2D sheet resistance for each nanosheet was calculated by summing the sheet resistances of constituent monolayers (Figure 2.1a,b):

$$R_{\mathrm{B}} = 1/\sum_{i=0}^{j-1} Q_i \mu_{\mathrm{B}} \text{ and } R_{\mathrm{T}} = 1/\sum_{i=j}^{j+k-1} Q_i \mu_{\mathrm{T}}$$

$$\text{(2.4)}$$

The 3D resistance of an elemental horizontal resistor with a mesh size L_{mesh} was then calculated as

$$R_{\mathrm{hor,B}} = R_{\mathrm{B}} \frac{L_{\mathrm{mesh}}}{W} \text{ and } R_{\mathrm{hor,T}} = R_{\mathrm{T}} \frac{L_{\mathrm{mesh}}}{W}$$

$$\text{(2.5)}$$

The mesh size was set to 1 nm for simulating micron-sized, experimentally fabricated junctions as in Figure 3.3, Figure 3.4, and Figure 3.5.

The intersheet tunneling was assumed to produce an effective resistance. Assuming that only carriers in neighboring monolayers at the interface contribute to tunneling at the interface, the effective intersheet carrier concentration was calculated as

$$Q_{\mathrm{int}} = \frac{Q_{j-1} + Q_j}{2}$$

$$\text{(2.6)}$$

where Q_j refers to the uppermost monolayer in the bottom nanosheet and Q_{j-1} refers to the bottommost monolayer in the top nanosheet (Figure 2.1a). The effective intersheet mobility μ_{int} was calculated by averaging the in-plane mobilities with anisotropy of 1000:[44]

$$\mu_{\text{int}} = \frac{\mu_{\text{T}} + \mu_{\text{B}}}{2} \frac{1}{1000} \tag{2.7}$$

The 3D intersheet resistivity was calculated as

$$\rho_{\text{int}} = \frac{d_{\text{int}}}{Q_{\text{int}} \mu_{\text{int}}} \tag{2.8}$$

where d_{int} is the intersheet distance, which was assumed to be equivalent to the monolayer thickness d_{ML}.

The resistance of an elemental vertical resistor was calculated as

$$R_{\text{ver}} = \rho_{\text{int}} \frac{d_{\text{int}}}{W} \frac{L_{\text{O}} + L_{\text{mesh}}}{L_{\text{O}} L_{\text{mesh}}} \tag{2.9}$$

where L_{O} is the length of the overlap.

Table 2.1. Summary of material constants

Parameter	Symbol	Value	References and Comments
Thickness of 1L MoS$_2$	d_{ML}	0.7 nm	
Dopant concentration	N_{3D}	10^{18} cm^{-3}	Typical value for our mechanically exfoliated MoS$_2$
SiO$_2$ permittivity	$\varepsilon_{\text{SiO2}}$	3.9	$C_{\text{ox}} = 1.21 \times 10^{-4}$ Fm^{-2} for 285 nm SiO$_2$
Out-of-plane permittivity 1L	ε_{OP}	$4.2\varepsilon_0$	[45] To calculate the λ_{OP} for gate screening, permittivity for the junction thickness was used (*i.e.*, for 1L/1L, ε_{OP} for 2L was used).
Out-of-plane permittivity 2L		$6.5\varepsilon_0$	
Out-of-plane permittivity bulk		$13.5\varepsilon_0$	
In-plane permittivity 1L	ε_{IP}	$2.8\varepsilon_0$	
In-plane permittivity 2L		$4.2\varepsilon_0$	
In-plane permittivity bulk		$8.5\varepsilon_0$	
Thermal conductivity 1L	κ	34.5 Wm^{-1}K^{-1}	[46] A temperature gradient $\nabla T = -Q/\kappa = 0.16$ Kμm^{-1} was calculated near the edge of 8L/8L, where $Q = IV/(Wt) = 5.8$ Wμm^{-2} is the power generated by the device.

2.1.3. Assigning Effective Edge Lengths and Near-Edge Resistivity Ratios

The larger near-edge resistances in the homojunction were considered by assigning effective edge lengths and near-edge resistivity ratios based on screening of charged impurities (Figure 2.2). The dominant mode of screening was determined by comparing the nanosheet thickness with the in-plane 2D and 3D Debye lengths.[38]

The in-plane 3D Debye length near both edges was calculated as

$$\lambda_{3D,E} = \sqrt{\frac{\varepsilon_E k_B T}{q^2 N_{3D}}} \tag{2.10}$$

where $\varepsilon_E = (\varepsilon_{IP} + \varepsilon_{OP})/2$ for mixed in-plane and out-of-plane screening of charges at edges. The 2D Debye length near the buried edge was calculated by considering screening of charges by the top MoS$_2$ and by SiO$_2$:

$$\lambda_{2D,BE} = \frac{k_B T}{q} \frac{\varepsilon_E + \varepsilon_{SiO2}}{q N_{2D}} \tag{2.11}$$

where $N_{2D} = t \times N_{3D}$. The 2D Debye length near the exposed edge was calculated by considering screening of charges by air and SiO$_2$:

$$\lambda_{2D,EE} = \frac{k_B T}{q} \frac{\varepsilon_{air} + \varepsilon_{SiO2}}{q N_{2D}} \tag{2.12}$$

For symmetric junctions with MoS$_2$ thicker than 6L, where the thickness is greater than all three Debye lengths, 3D screening dominates near both edges, resulting in an effective buried edge length $L_{BE} = t$ and an exposed edge length $L_{EE} = \lambda_{3D,E}$ (Figure 2.2a). For MoS$_2$ thinner than 4L, where the thickness is smaller than all three Debye lengths, 2D screening dominates near both edges, resulting in $L_{BE} = \lambda_{2D,BE}$ and $L_{EE} = \lambda_{2D,EE}$ (Figure 2.2b). For 4L-5L MoS$_2$, where $\lambda_{2D,EE} < t <$

$\lambda_{3D,E} < \lambda_{2D,BE}$, 2D screening dominates near the BE while 2D and 3D screening effects are mixed near the EE, resulting in $L_{BE} = \lambda_{2D,BE}$ and $L_{EE} = (\lambda_{2D,EE} + \lambda_{3D,E})/2$ (Figure 2.2c). For 6L MoS$_2$, where $\lambda_{2D,EE} < \lambda_{3D,E} < t < \lambda_{2D,BE}$, 2D and 3D screening effects are mixed near the BE while 3D screening dominates near the EE, resulting in $L_{BE} = (\lambda_{2D,BE} + \lambda_{3D,E})/2$ and $L_{EE} = \lambda_{3D,E}$ (Figure 2.2d). For asymmetric junctions, the Debye lengths and thus edge lengths were evaluated separately for top and bottom nanosheets.

For symmetric junctions with MoS$_2$ thicker than 5L, 3D screening dominates near the EE, resulting in complete screening of charges by the bottom nanosheet (*e.g.*, 8L/8L) and thus weak perturbation of its resistivity $R_{B,EE}/R_B = 1$. For symmetric junctions with 1L-5L MoS$_2$, near-edge resistivity ratios where $R_{T,BE}/R_T = R_{T,EE}/R_T = R_{B,BE}/R_B = R_{B,EE}/R_B = 10^3$ and $\rho_{i,BE}/\rho_i = \rho_{i,EE}/\rho_i = 1$ were assigned to both nanosheets near both edges. For the 5L/1L, $R_{T,BE}/R_T = 1$ was assigned for the t-5L near the BE to account for the negligible potential drop.

The Debye lengths, effective edge lengths, and near-edge resistivities are summarized in Table 2.2. The sheet resistances and intersheet resistivity values for regions within the identified effective edge lengths were then increased accordingly when constructing the model.
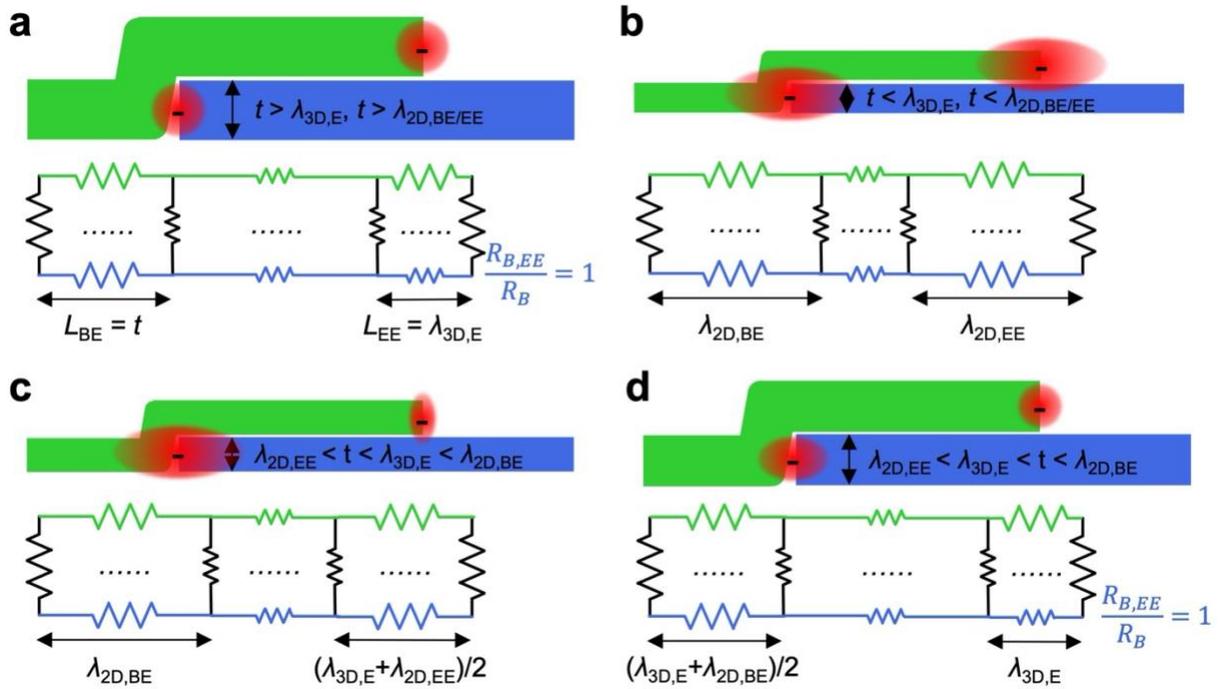
Figure 2.2. Schematics for assigning effective edge lengths and near-edge resistivity ratios to homojunctions with different thicknesses. Here the horizontal resistors represent the total sheet resistance.

Table 2.2. Summary of Debye lengths, effective edge lengths, and near-edge resistivity ratios for MoS₂/MoS₂.

Junction	t (nm)	λ_{OP} (nm)	$\lambda_{3D,E}$ (nm)	$\lambda_{2D,BE}$ (nm)	$\lambda_{2D,EE}$ (nm)	L_{BE} (nm)	L_{EE} (nm)	$R_{T,BE}/R_T =$ $R_{T,EE}/R_T =$ $R_{B,BE}/R_B$	$R_{B,EE}/R_B$	$\rho_{i,BE}/\rho_i =$ $\rho_{i,EE}/\rho_i$
1L/1L	0.7	3.1	2.2	15.2	10.1	15.2	10.1	1000	1000	1
2L/2L	1.4	4.4	2.8	9.5	5.0	9.5	5.0	1000	1000	1
3L/3L	2.1	4.4	4.0	10.2	3.4	10.2	3.4	1000	1000	1
4L/4L	2.8	4.4	4.0	7.7	2.5	7.7	3.2	1000	1000	1
5L/5L	3.5	4.4	4.0	6.1	2.0	6.1	3.0	1000	1000	1
6L/6L	4.2	4.4	4.0	5.1	1.7	4.5	4.0	1000	1	1
7L/7L	4.9	4.4	4.0	4.4	1.4	4.9	4.0	1000	1	1
8L/8L	5.6	4.4	4.0	3.8	1.3	5.6	4.0	1000	1	1
9L/9L	6.3	4.4	4.0	3.4	1.1	6.3	4.0	1000	1	1
10L/10L	7.0	4.4	4.0	3.1	1.0	7.0	4.0	1000	1	1
11L/11L	7.7	4.4	4.0	2.8	0.9	7.7	4.0	1000	1	1
12L/12L	8.4	4.4	4.0	2.6	0.8	8.4	4.0	1000	1	1
13L/13L	9.1	4.4	4.0	2.4	0.8	9.1	4.0	1000	1	1
14L/14L	9.8	4.4	4.0	2.2	0.7	9.8	4.0	1000	1	1
15L/15L	10.5	4.4	4.0	2.0	0.7	10.5	4.0	1000	1	1
5L/1L	3.5/0.7	4.4	4.0/2.2	6.1/3 0.6	2.0/1 0.1	6.1/3 0.6	3.0/1 0.1	$R_{T,EE}/R_T =$ $R_{B,BE}/R_B =$ $R_{B,EE}/R_B =$ 50000	$R_{T,BE}/R_T$ = 1	250

Note: For symmetric junctions, the sheet resistance ratios ($R_{S,E}/R_S$ and $R_{B,EE}/R_B$) and intersheet resistivity ratios ($\rho_{i,E}/\rho_i$) are given as the values used to simulate Figure 3.7, Figure 3.8, and Figure 3.9.

2.1.4. Simulating Printed Films with Multiple Stacks of Nanosheets

To simulate the performance of printed films with stacks of nanosheets, we assume that the nanosheets are sufficiently large and thin (*i.e.*, length/thickness > 40 for MoS₂)[30] to form conformal junctions with mostly buried edges (Figure 2.3a).

For each stack of nanosheets at the junction, a series of three horizontal resistors represents the intrasheet (in-plane) resistances in the middle of the junction (R_X) and near the edges ($R_{X,E}$ and

$R_{1,EE}$). The resistance R_X for the Xth stack of sheet was calculated based on the gate-dependent carrier concentration model described above (Figure 2.1). The near-edge resistance ratios ($R_{X,E}/R_X$, $R_{1,EE}/R_1$, and $\rho_{i,E}/\rho_i$) and the effective buried edge length (L_{BE}) were assigned for different nanosheet thicknesses based on Table 2.2. The resistance outside of the junction was calculated by assuming that the current is only carried by the parallel sheets.
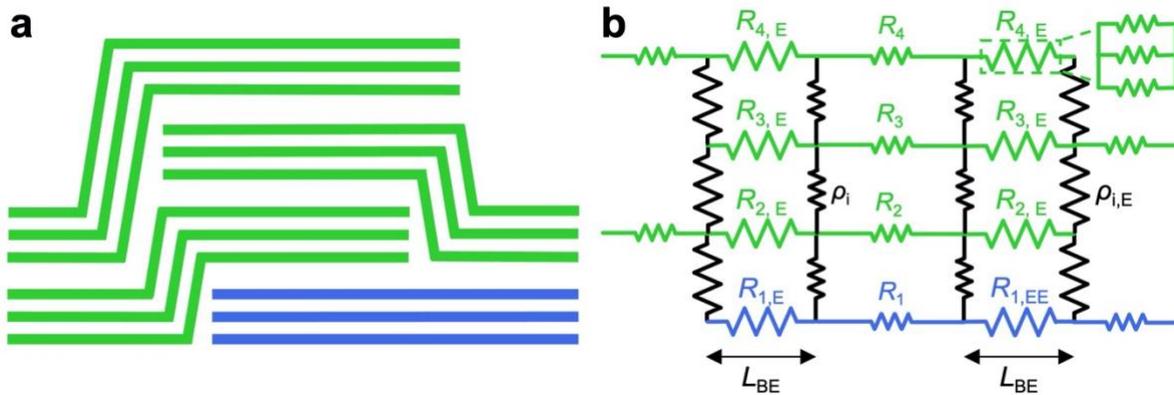
Figure 2.3. (a) Schematic and (b) resistor network model for multiple stacks of nanosheets.

2.1.5. Solving the Resistor Network

The Kirchhoff law states that $L\vec{V} = \vec{I}$, where L is the Laplacian matrix associated with the network, which takes the general form:

$$L = \begin{bmatrix} C_1 & -C_{12} & \cdots & -C_{1N} \\ -C_{21} & C_2 & \cdots & -C_{2N} \\ \vdots & \cdots & \ddots & \vdots \\ -C_{N1} & -C_{N2} & \cdots & C_N \end{bmatrix}$$

(2.13)

where $C_i \equiv \sum_{j=1}^{N} C_{ij}$.

The Laplacian was solved for the non-zero eigenvalues λ_i and orthogonal eigenvalues φ_i. Then the resistance between nodes α (bias location) and β (ground location) was given by[47]

$$R_{\alpha\beta} \; = \; \sum_{i=2}^{N} \frac{1}{\lambda_i} \left| \varphi_{i\alpha} - \varphi_{i\beta} \right|^2$$

(2.14)

The potential at each node γ was calculated by

$$V_\gamma - V_\beta \; = \; I \sum_{i=2}^{N} \frac{1}{\lambda_i} (\varphi_{i\gamma} - \varphi_{i\beta})(\varphi_{i\alpha}^* - \varphi_{i\beta}^*)$$

(2.15)

For the two-nanosheet system, a 2M×2M Laplacian matrix was constructed (Figure 2.4a), where M-1 is the number of meshes for the junction; the junction resistance was calculated between M-1 (ground) and M. For simulating printed films with multiple stacks of nanosheets, a (4X-1)×(4X-1) Laplacian matrix was constructed (Figure 2.4b), where X is the number of stacked nanosheets at junction; the junction resistance was calculated between 3X+1 (ground) and X-1. The resistances in the middle of the junction and near the edges were converted to conductances and assigned to the corresponding matrix elements.
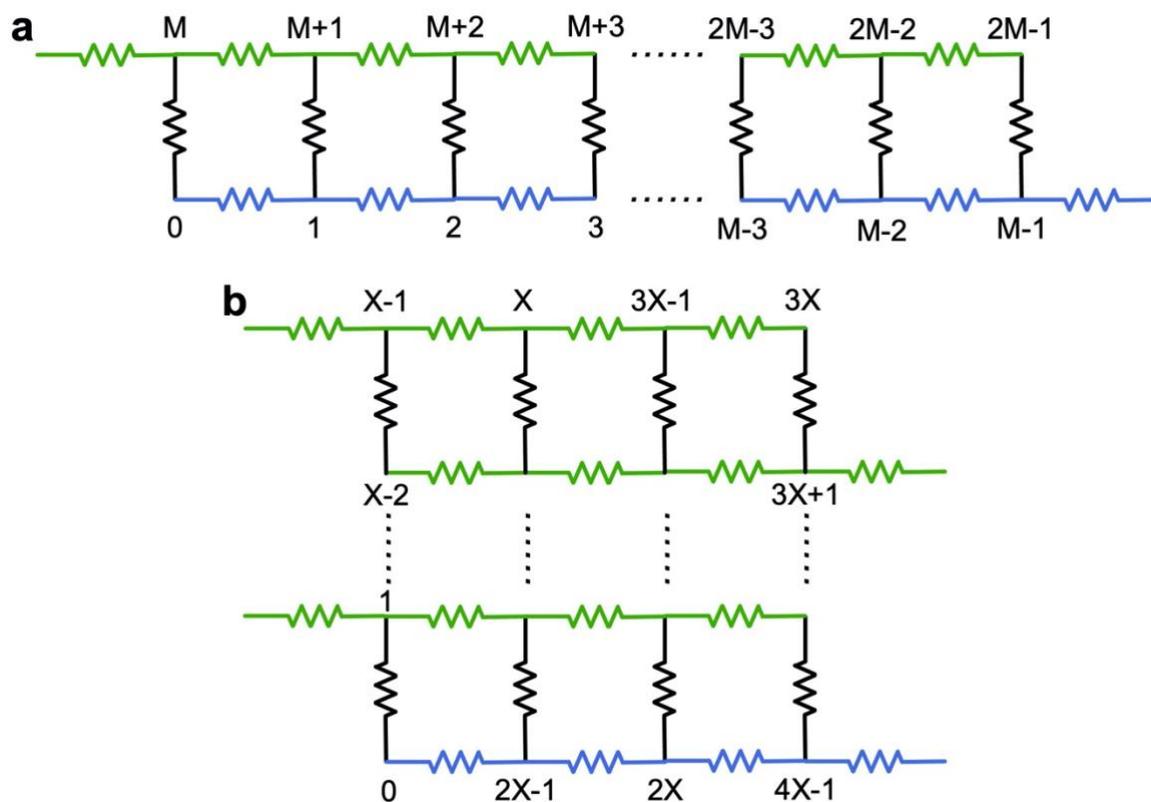
Figure 2.4. Schematic for constructing the Laplacian matrix associated with resistor network for (a) two-nanosheet system and (b) printed films with multiple stacks of nanosheets.

2.2. Y-function Analysis of Transfer Curves

The drain-source current in strong accumulation (Figure 3.2 and Figure 5.5), when the transconductance saturates or decreases, was modeled as[48]

$$I_{DS} = \frac{W}{L}C_{ox}(V_{GS} - V_{TH})\frac{\mu_0}{1 + \theta(V_{GS} - V_{TH})}V_{DS}$$

(2.16)

where I_{DS} is the drain-source current, V_{DS} is the drain-source voltage, W is the channel width, L is the channel length, C_{ox} is the capacitance of the gate dielectric, V_{GS} is the gate-source voltage, V_{TH} is the threshold voltage, μ_0 is the intrinsic mobility of the channel, and θ is the mobility attenuation factor. The expression assumes that the access resistance is constant and that the channel resistance is controlled by the gate. The access resistance R_A, which refers to the resistance that arises due to the presence of parasitic elements within the device, was calculated from the extracted μ_0 and θ as

$$R_A = \frac{\theta}{\mu_0}\frac{L}{WC_{ox}}$$

(2.17)

The contact and junction resistances for the 8L/8L device were then estimated from R_A (Chapter 3 Section 3.8.1).

For devices in which the transconductance does not saturate or decrease (Figure 3.12, Figure 3.13, and Figure 5.4), the field-effect mobilities $\mu_{FE} = (dI_{DS}/dV_{GS})(L/V_{DS}WC_{ox})$ were extracted at a particular V_{GS}, assuming that transport is limited by the channel resistance instead of the contact resistance.

2.3.   *Operando* Kelvin Probe Force Microscopy

In Chapter 3, *operando* Kelvin probe force microscopy (KPFM) was used to measure the spatially resolved surface potential profiles of the MoS_2/MoS_2 model transistors under bias.

2.3.1.   KPFM Principles, Operation Modes, and Resolutions

The KPFM is a non-contact AFM-based technique that measures the contact potential difference (V_{CPD}) between a conducting tip and the sample surface:[49]

$$V_{CPD} = \frac{\Phi_t - \Phi_s}{-e}$$

$$\text{(2.18)}$$

where Φ_t and Φ_s are the work functions of the tip and the sample, and e is the elementary charge.

When the tip and sample are electrically isolated and separated by a distance, their vacuum levels are aligned but the Fermi levels are different, exhibiting a work function difference (Figure 2.5a). When the tip and sample are electrically connected and brought into close proximity (but not in contact), electrons will flow from the one with a lower work function to the one with a higher work function to align their Fermi levels, equal and opposite charges will be induced on the surfaces, and a contact potential difference will form, which is equal to the work function difference (Figure 2.5b). To measure the V_{CPD}, the tip is modulated at a specific frequency by applying an AC bias (V_{AC}) that induces an oscillating electrostatic force. A backing DC voltage (V_{DC}) that is equal and opposite to the V_{CPD} is applied to nullify the force, either in the amplitude-modulated (AM) mode or the frequency-modulated (FM) mode (Figure 2.5b).
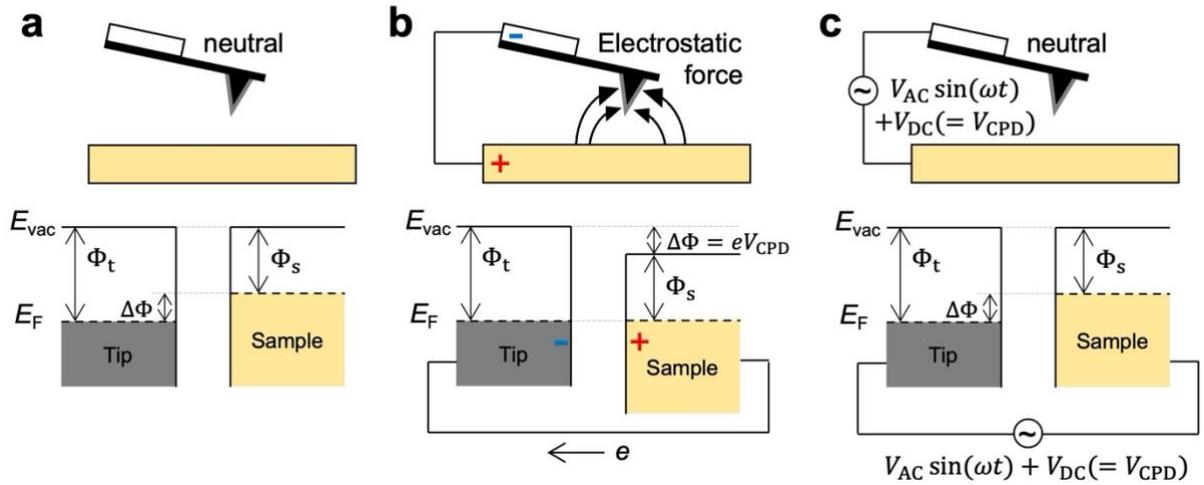
Figure 2.5. Kelvin probe force microscopy (KPFM) principles. Schematics illustrating the electrostatic interaction (top) and energy levels (bottom) of tip and sample for three cases: (a) tip and sample are electrically isolated and physically separated, (b) tip and sample are electrically connected and develop a contact potential difference (V_{CPD}) that is equal to the work function difference ($\Delta\Phi$), and (c) a DC voltage (V_{dc}) is applied between tip and sample to nullify the V_{CPD} and thus the tip-sample electrostatic force. E_{vac} is the vacuum energy level. E_F is the Fermi level. Credit to Dr. Alex Henning.

The electrostatic force F_{el} applied to the AFM tip is:[50]

$$F_{el} = \frac{-1}{2}\frac{\partial C}{\partial z}(\Delta V)^2$$

(2.19)

where $\partial C/\partial z$ is the capacitance gradient.

The voltage difference created between the tip and the sample is:[50]

$$\Delta V = V_{DC} - V_{CPD} + V_{AC}\sin(\omega t)$$

(2.20)

Hence, there are three terms for the F_{el}, the DC term (F_{DC}), the ω term (F_ω), and the 2ω term ($F_{2\omega}$):[50]

$$F_{DC} = \frac{\partial C}{\partial z}\left((V_{DC} - V_{CPD})^2 + \frac{1}{2}V_{AC}^2\right)$$

(2.21)

$$F_\omega = \frac{\partial C}{\partial z}(V_{DC} - V_{CPD})V_{AC}\sin(\omega t)$$

(2.22)

$$F_{2\omega} = \frac{1}{4}\frac{\partial C}{\partial z}V_{AC}{}^2\cos(2\omega t)$$

(2.23)

The electrostatic force gradient is associated with the force via $F_{el}' = \partial F_{el}/\partial z$, similarly having

three components:[50]

$$F_{DC}' = \frac{\partial^2 C}{\partial z^2}((V_{DC} - V_{CPD})^2 + \frac{1}{2}V_{AC}{}^2)$$

(2.24)

$$F_\omega' = \frac{\partial^2 C}{\partial z^2}(V_{DC} - V_{CPD})V_{AC}\sin(\omega t)$$

(2.25)

$$F_{2\omega}' = \frac{1}{4}\frac{\partial^2 C}{\partial z^2}V_{AC}{}^2\cos(2\omega t)$$

(2.26)

In AM-KPFM, an AC bias is applied between the tip and the sample at the resonance

frequency to modulate the electrostatic force (Equation 2.22), which modulates the oscillation

amplitude of the cantilever. The KPFM feedback, using the oscillation amplitude as the input,

adjusts the DC bias until the oscillation amplitude drops to 0, when V_{DC} equals V_{CPD}.

In Chapter 3, we utilized the Bruker PeakForce KPFM configuration, which employs the FM-

KPFM mode to modulate the force gradient by modulating the resonance frequency. This method

provides higher spatial resolution than the AM-KPFM mode. A typical force vs. distance curve is

shown in Figure 2.6a. In the attractive force regime, the force gradient (the derivative of the force-

distance curve) becomes larger as the distance between the tip and the sample decreases. However,

as the distance increases, the force gradient becomes negligible. Hence, the detection of the force

gradient primarily occurs at the end of the AFM tip (*i.e.*, the tip cone).

The force gradient changes the effective spring constant k_{eff}:[50]

$$k_{\text{eff}} = k - \frac{\partial F_{\text{el}}}{\partial z}$$

(2.27)

where k is the original spring constant.

Thus, the modulation of the resonance frequency:[50]

$$\Delta\omega = \omega_{\text{eff}} - \omega = \sqrt{\frac{k_{\text{eff}}}{m}} - \sqrt{\frac{k}{m}} \approx \frac{-\omega}{2k}\left(\frac{\partial F_{\text{el}}}{\partial z}\right)$$

(2.28)

where ω is the original resonance frequency and ω_{eff} is the effective resonance frequency after modulation.

In FM-KPFM, the tip is *mechanically oscillated* at its resonance frequency ω, while a small AC bias of frequency ω_{m} is applied to excite the AC electrostatic force F_{ω}, resulting in modulation of the resonance frequency by:[50]

$$\Delta\omega \approx \frac{-\omega}{2k} F_{\omega_{\text{m}}}{}' \equiv F_{\text{m}} \sin(\omega_{\text{m}} t)$$

(2.29)

where F_{m} is the frequency modulation amplitude.

Two pairs of sidebands are created for the cantilever deflection with respect to its resonance frequency at $\omega \pm \omega_{\text{m}}$ (Equation 2.25) and $\omega \pm 2\omega_{\text{m}}$ (Equation 2.26), as shown in Figure 2.6b. The ratio of the sum of the first $\omega \pm \omega_{\text{m}}$ sidebands versus the center peak height gives the frequency modulation index $F_{\text{m}}/\omega_{\text{m}}$ for the potential feedback, which adjusts the DC bias until the pair of sidebands disappears, where V_{DC} equals V_{CPD}.

The FM-KPFM instrumentation involves two cascade lock-in amplifiers to separately lock the resonance ω and sideband ω_{m} frequencies for the potential feedback (Figure 2.6c). The

representative settings (Lock-In2 and Lock-In3) are shown in Figure 2.6d. (The Lock-In1 in Figure 2.6d is for setting the topography feedback.) The first lock-in amplifier (Lock-In2 settings) uses the photodiode deflection as input, locks the resonance frequency ω (Drive Frequency = Drive2 Frequency = 81.2 kHz), and outputs the phase shift at the resonance frequency to the 2nd lock-in amplifier. Note that the internal oscillator in Lock-In2 is turned off (Drive2 Amplitude = 0 mV), as the drive amplitude for the cantilever has already been set during the topography measurements. For a small modulation ($F_m/\omega_m < 0.2$), the phase shift ϕ is related to the frequency modulation amplitude F_m by[50]

$$\phi \approx \frac{F_m}{\omega_m} \sin(\omega_m t)$$

(2.30)

The second lock-in amplifier (Lock-In3 settings) uses ϕ as input, locks the frequency of the applied AC bias ω_m (Drive3 Frequency = 2.0 kHz, Figure 2.6d), and outputs the modulation amplitude of the $\omega \pm \omega_m$ sidebands. The KPFM feedback loop takes the amplitude as input and adjusts the DC bias until the amplitude drops to zero (*i.e.*, the sidebands disappear). Typically, the tip is grounded, and the bias is applied to the sample/stage (Tip Bias = 0 V, Drive2 Routing = Sample).

The topography and potential were measured in a dual-pass fashion using lift mode, where the topography was measured first, and then the tip was lifted to a certain height to measure the potential. To ensure stable imaging, the scan rate for both topography and potential measurements should be slower than the transient time response of the feedback loop. The lift height (Lift Scan Height in Interleave settings, Figure 2.6d) should be chosen as the minimum height that maintains a stable imaging condition. A larger lift height increases the contribution of the cantilever to the overall signal, thus decreasing the spatial resolution of the potential measurement. Setting the lift

height too small can cause the tip to directly contact the sample surface, leading to abrupt phase

changes that destabilize the potential feedback loop with finite bandwidth.
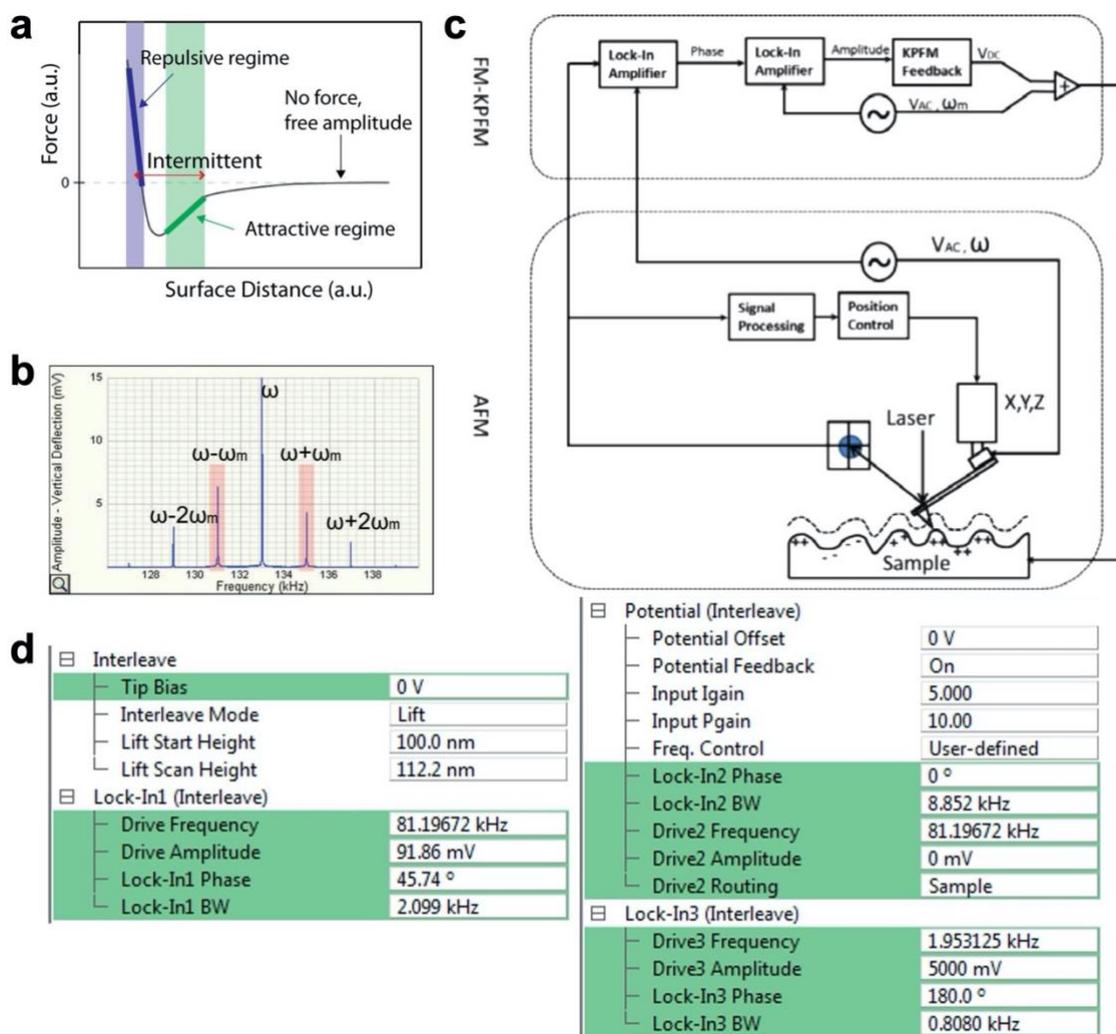
Figure 2.6. FM-KPFM principles, instrumentation, and settings. (a) A typical force vs. surface distance curve. (b) Amplitude vs. frequency of the cantilever deflection by oscillating at its resonance frequency ω while applying an AC bias of ω_m, illustrating the emergence of sidebands. (c) Instrumentation of FM-KPFM that involves two cascade lock-in amplifiers. (d) Representative settings for the PeakForce KPFM configuration in Bruker Dimension Icon AFM. Credit to Bruker Nano Surfaces.[50]

The spatial resolution of KPFM at a constant lift height can be approximated by scanning across an atomically sharp edge. The spatial resolution of the KPFM measurements in Chapter 3 was estimated to be ~300 nm from the lateral spread in the CPD profile near the exposed edge of the top-5L on top of the bottom-1L (Figure 2.7). The energy resolution for FM-KPFM has been reported to be 10 mV.[49]
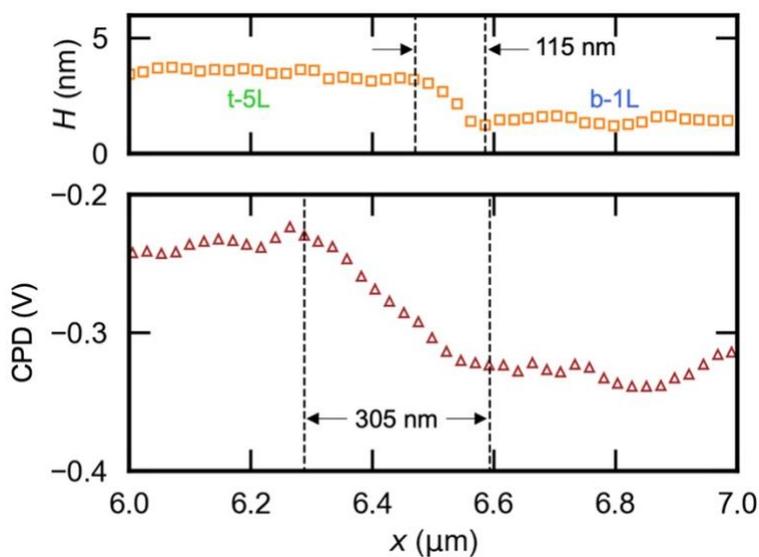
Figure 2.7. Estimating spatial resolution of KPFM near the exposed edge of 5L/1L. The tip was lifted 180 nm from the sample surface when measuring the CPD.

2.3.2. *Operando* KPFM Measurement Set-up

In addition to measuring the work function of a sample in equilibrium, KPFM can be used to measure the surface potential of an electronic device while it is under bias, known as *operando* KPFM.[1,43,51–54] By simultaneously recording the current, the resistances of the channel and across the junctions of the device can be calculated, providing a mechanistic understanding of the device's operation.

The KPFM measurements in Chapter 3 were carried out in ambient with a Bruker Dimension Icon AFM. The device was connected to a custom chip carrier via wedge bonding (Figure 2.8). LabVIEW-controlled Keithley 2400 source measure units (SMUs) were used to apply drain-source (V_{DS}) and gate-source (V_{GS}) biases to the devices and to measure the device current during KPFM (Figure 2.8 inset). The height H and contact potential difference V_{CPD} profiles were sequentially measured (*i.e.*, lift mode) using the PeakForce KPFM configuration. For measuring the MoS_2/MoS_2 model transistors, the Pt/Ir-coated conductive tips (NanoAndMore PPP-EFM) were scanned at a rate of 0.1 Hz and lifted 180 nm from the sample surface to avoid contact with features at the contact edges.

To ensure precise potential measurements of the device at the tip cone, several factors must be carefully considered. First, the fast scan direction should primarily be along the channel length to ensure that the tip is symmetrical along the scan direction. Second, the cantilever should have minimal overlap with conductive features outside the scan window to reduce the influence of parasitic capacitance between the cantilever and the substrate on the signal at the tip cone. Lastly, when measuring the potential of a device fabricated on a local gate, the global bottom gate (usually

the Si substrate) should be grounded to prevent the floating potential from interfering with the

measured device potential.
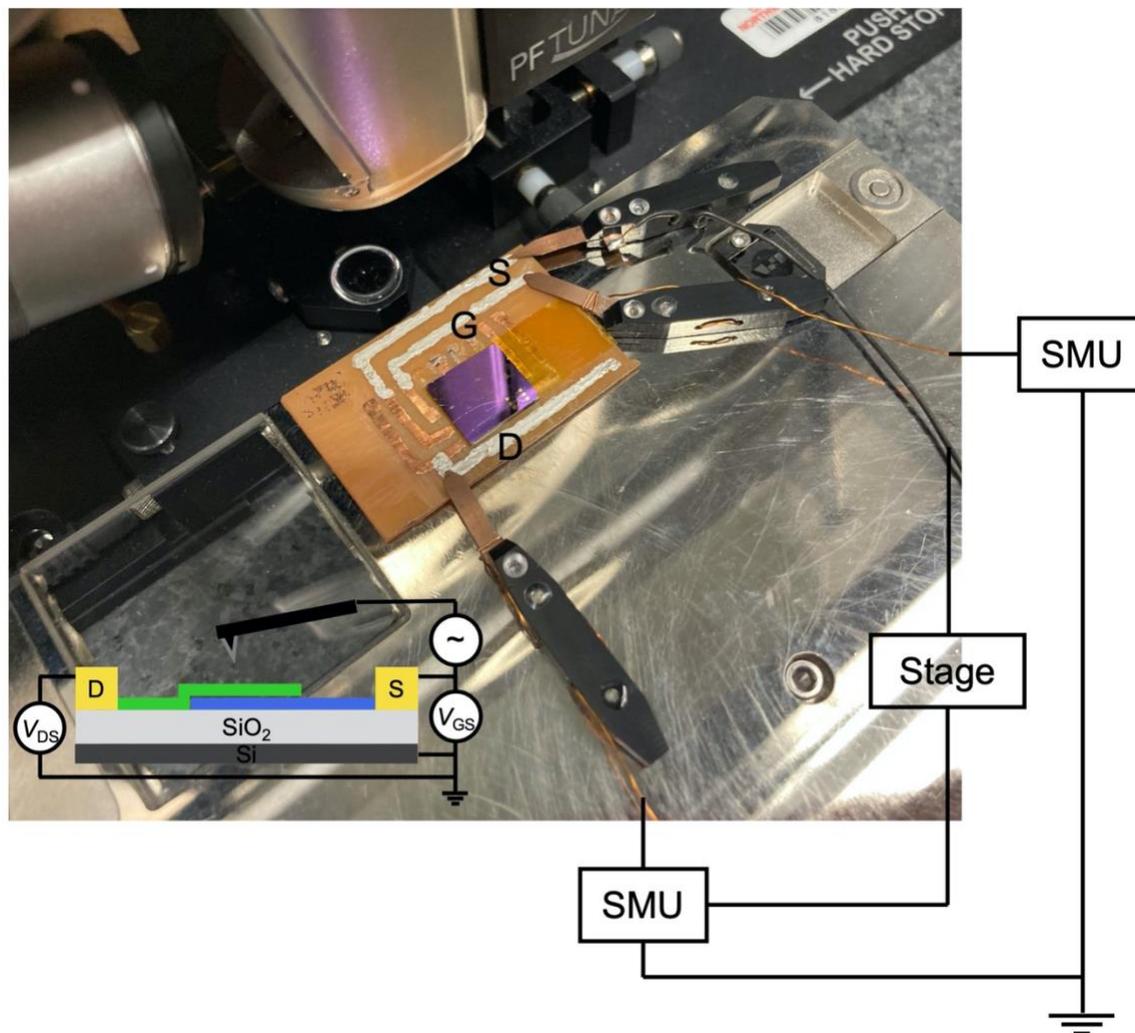
Figure 2.8. *Operando* **KPFM set-up. Actual and schematic (inset) connections used to measure the surface potential profile of a device under bias.**

2.3.3. Extracting Conductivity from Potential Profile

For each V_{GS}, the V_{CPD} under $V_{DS} = 0$ V (*i.e.*, equilibrium) was subtracted from the V_{CPD} under

nonzero V_{DS}. Figure 2.9 shows the equilibrium, $V_{DS} = 1$ V, and the subtracted V_{CPD} for the 8L/8L

device. The subtracted CPD was fitted by Ohm's law to extract the conductivity:

$$\frac{I_{DS}}{W} = \sigma t E = G_S \frac{dV_{CPD}}{dx}$$

(2.31)

where I_{DS} is the drain-source current, W is the channel width, σ is the conductivity, t is the channel

thickness, E is the electric field, and G_s is the sheet conductance.
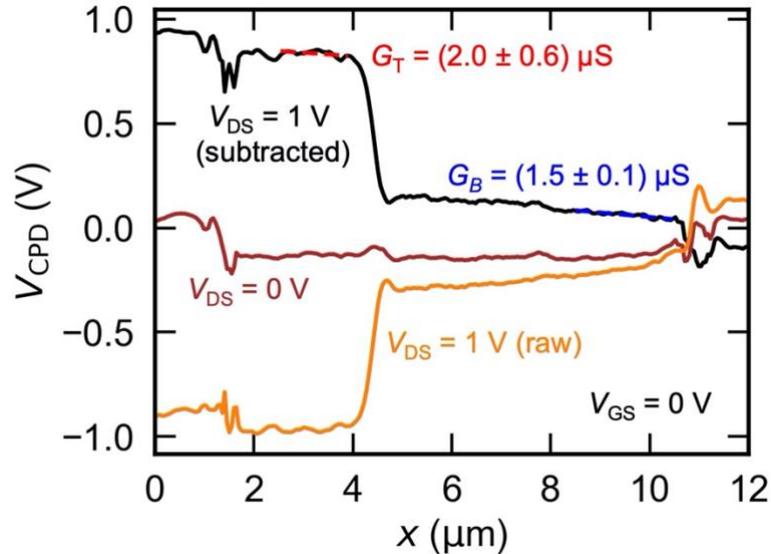
Figure 2.9. Extracting sheet conductance for the 8L/8L device. V_{CPD} **vs. position** x **profile at** $V_{DS} = 0$ **V (brown) was subtracted from the profile at** $V_{DS} = 1$ **V (orange) to obtain the black line. The sheet conductances** G_T **and** G_B **were then extracted for the top and bottom nanosheets by performing linear fits (red and blue dashed lines).**

2.4. Impedance Spectroscopy

Chapter 4 Section 4.3 utilized impedance spectroscopy to investigate the photoresponse origins of printed MoS_2 photodetectors.

2.4.1. Impedance Analyzer Working Principles and Instrument Limitations

A Solartron Analytical 1260 impedance analyzer was used to measure the electrical impedance. It consists of a signal generator and an analyzer (Figure 2.10a). The generator produces an AC voltage of known frequency and amplitude, while the analyzer uses a lock-in amplifier to measure the amplitude and phase of the differential voltage ($\tilde{V}$) across the item under test (IUT) and the current ($\tilde{I}$) at each frequency, from which the impedance (Z) is calculated:[55]

$$Z(\omega) = \frac{\tilde{V}(\omega)}{\tilde{I}(\omega)} = \left|\frac{\tilde{V}(\omega)}{\tilde{I}(\omega)}\right| (\cos \phi(\omega) + j \sin \phi(\omega)) = Z^{\text{R}}(\omega) + jZ^{\text{I}}(\omega)$$

$$(2.32)$$

where the angular frequency ω relates to the frequency f by $\omega = 2\pi f$, ϕ is the phase angle between the voltage and current, and Z^{R} and Z^{I} are the real and imaginary components of the complex impedance.

The instrument can measure up to 100 MΩ with a 10% error at frequencies below 1 kHz (Figure 2.10b). However, at 1 MHz, the measurement limitation decreases to 1 MΩ, which is equivalent to 0.16 pF for a pure capacitor (Figure 2.10a). Note that for a pure capacitor, $Z = 1/(j\omega C)$ with a -90° phase shift (*i.e.*, the voltage lags the current by 90°), where C is the capacitance.
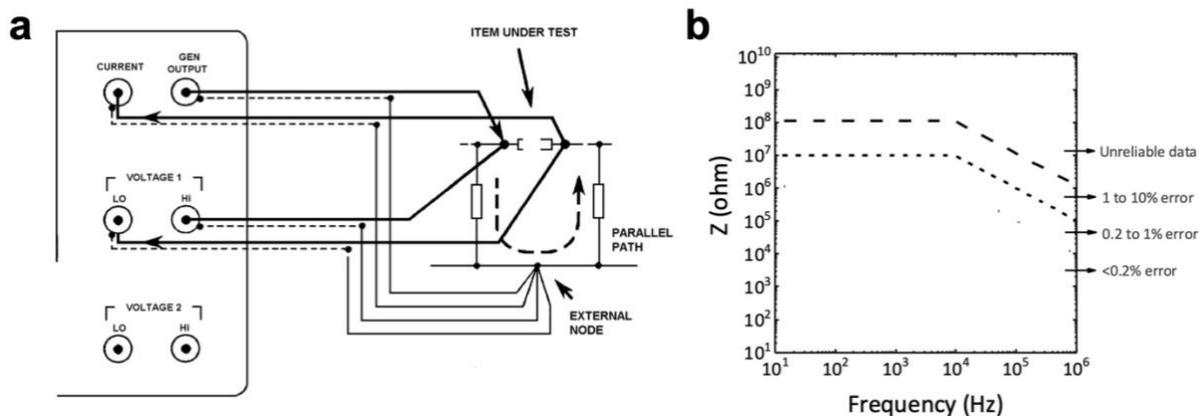
Figure 2.10. Impedance measurement setup and instrument limitations. (a) Connections that are made for the impedance measurements. (b) Maximum measurable impedance *Z* vs. frequency for the Solartron Analytical 1260 impedance analyzer with different accuracies, reproduced from the manual.

2.4.2. Minimizing Parasitic Capacitance with Shielded Connectors

To minimize the impact of parasitic capacitance on the measurable impedance of the device under test (IUT), shielded cables and connectors that have a common conductive layer around the conducting core are necessary. Figure 2.11a compares the impedance measured using cables with shielded BNC connectors and unshielded alligator clips (Figure 2.11b). The BNC connectors produce higher impedance values compared to the alligator clips. The capacitances of the cables were extracted by linear fitting the impedance at higher frequencies, resulting in 0.3 pF for the BNC connectors and 12 pF for the alligator clips. Since parasitic capacitance is in parallel with the sample (Figure 2.11c), having a smaller parasitic capacitance increases the measured capacitance relative to the parasitic capacitance, thus increasing the measurability of the IUT. Figure 2.11a shows that when measuring a standard 4.7 pF capacitor, the measured impedance decreases by 10

times when using cables with BNC connectors, while only marginally when using the alligator clips.
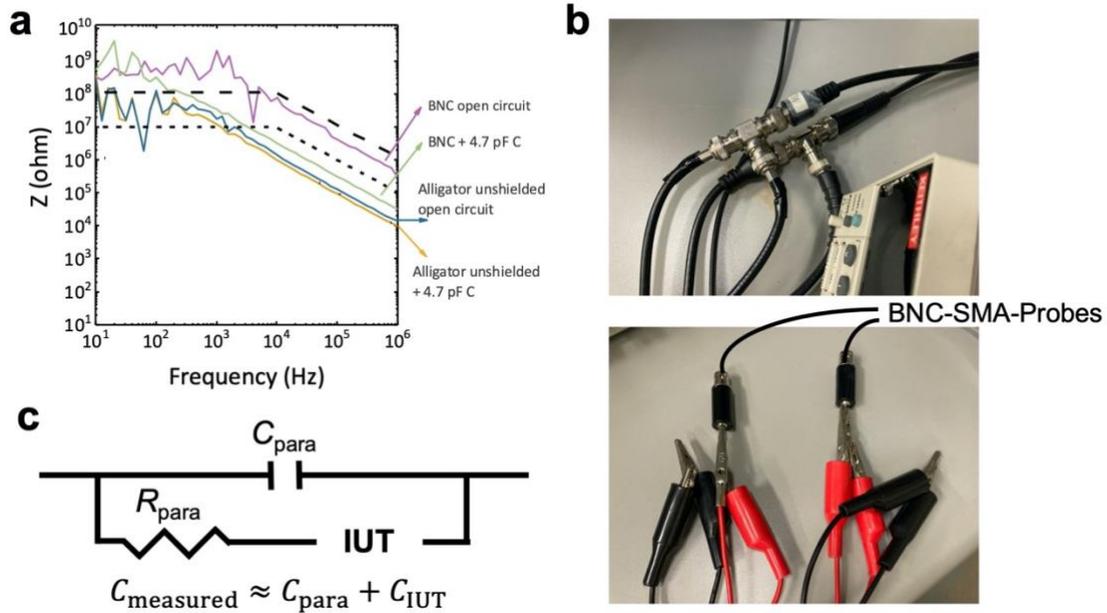
Figure 2.11. Impedance measurements with different connectors. (a) Impedance vs. frequencies of a 4.7 pF standard capacitor, measured using cables with BNC connectors and alligator clips. (b) Pictures of cables with BNC connectors (top) and alligator clips (bottom). (c) Equivalent circuit for typical impedance measurement,[55] where the item under test (IUT) is in parallel with the parasitic capacitance.

2.5. Atomic Layer Deposition Growth

Atomic layer deposition (ALD) growth of SnS_2 and SnO_x enabled work presented in Chapter 5 Section 5.3.

2.5.1. ALD SnS$_2$

The ALD recipe for growing SnS_2 for the work detailed in Section 5.3.1 is shown in Figure 2.12. The recipe was developed by Dr. Michael Moody. The growth chamber was maintained at 150 °C. Before SnS_2 growth, the printed MoS_2 devices were treated with O_3 at ~2 torr for 10 min, followed by H_2S at ~1 torr for min. For the SnS_2 growth, each growth cycle consists of 2 sequential 1 s pulses of $Sn[(CH_3)_2N]_4$ precursor and 3 sequential 1 s pulses of H_2S, with 20 s purge between each pulse. Ellipsometry measurements performed by Dr. Lee J. Richter from NIST showed that 200 growth cycles produced 8 nm SnS_2 on printed MoS_2.
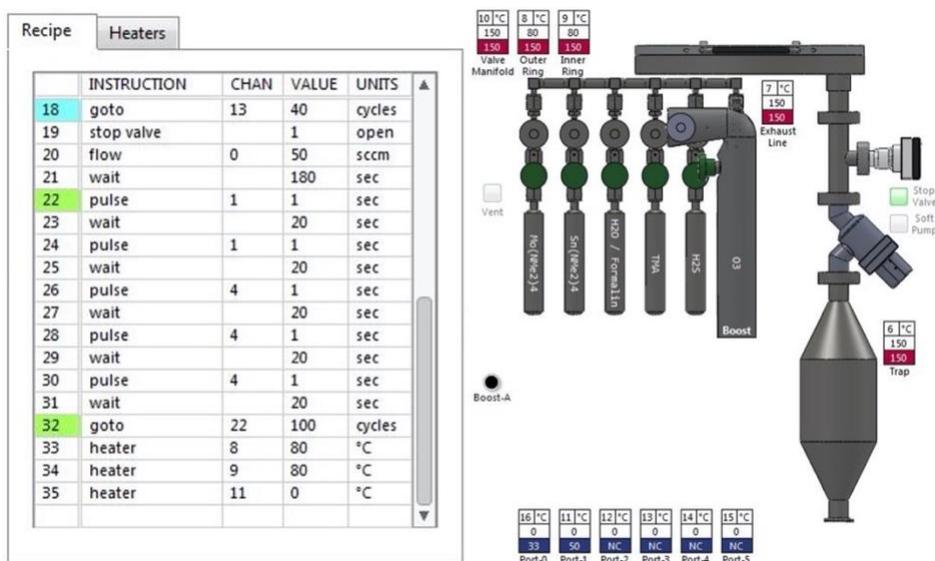
Figure 2.12. Atomic layer deposition (ALD) growth recipe of SnS$_2$ for Section 5.3.1. Detailed information for the run can be found: 20191107_SnS$_2$-insitu.

2.5.2. ALD SnO_x for In Situ Transport Measurement

The ALD recipe for growing SnO_x for the work detailed in Section 5.3.2 is shown in Figure 2.13a. The growth chamber was maintained at 80 °C. Each growth cycle consists of a 5 s pulse of $Sn[(CH_3)_2N]_4$ precursor at 50 °C and 0.1 s pulse of H_2O, with 30 s purge between each pulse. For *in situ* measurement of transfer curves during growth, the process was paused for 10 min after every 5 cycles. For patterning SnO_x on exfoliated MoS_2 nanosheets, the growth continued without pausing.

To calibrate the thickness measured by the quartz crystal monitor (QCM), SnO_x strips grown at various numbers of cycles were patterned on 7L-MoS_2 nanosheets using a standard S1805 photolithography. The thicknesses of these strips were measured with AFM. The SnO_x thickness measured on MoS_2 was then correlated with the QCM thickness (Figure 2.13b), allowing for *in situ* calibration of the SnO_x thickness (Figure 2.13c and Figure 5.5).

Figure a — Recipe table:

	INSTRUCTION	CHAN	VALUE	UNITS
0	flow	0	20	sccm
1	wait		560	sec
2	pulse	1	5	sec
3	wait		30	sec
4	pulse	2	0.1	sec
5	wait		30	sec
6	goto	2	5	cycles
7	wait		600	sec
8	goto	2	20	cycles

Precursor #1: $Sn[(CH_3)_2N]_4$
Precursor #2: H_2O

slope = 1.36 ± 0.03
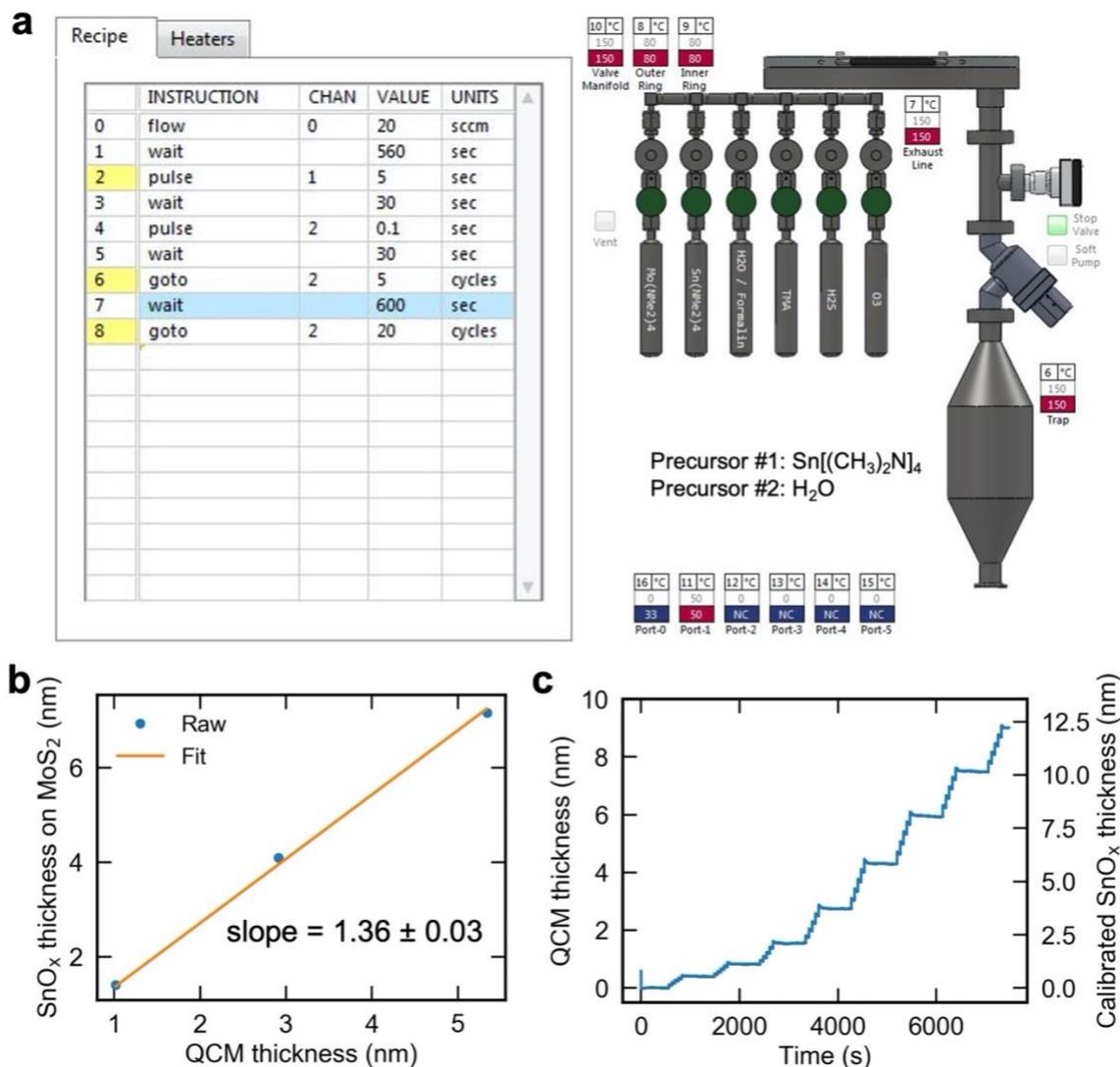
Figure 2.13. ALD SnOₓ growth calibration. (a) ALD SnOₓ growth recipe for Section 5.3.2. Detailed information for the run can be found: 20190319_SnO-insitu. (b) SnOₓ thickness measured on 7L MoS₂ by AFM vs. QCM thickness. (c) QCM thickness and calibrated SnOₓ thickness during the *in situ* transport measurement (Section 5.3.2 Figure 5.5).

2.6. Device Fabrication

Processes were developed to fabricate devices for the work in Chapter 3, MoS_2/MoS_2 homojunction FETs (Section 2.6.1), and for the work in Chapter 6, electrolyte-gated transistors (Section 2.6.2).

2.6.1. Fabrication of MoS₂/MoS₂ Homojunction FETs

MoS_2 crystals (HQ Graphene) were mechanically exfoliated onto clean n^+-Si/SiO₂ (285 nm) substrates by heating the Scotch tape/substrate at 90 °C for 15 min before releasing the tape.[56] Tape residues were removed by soaking in acetone at 40 °C for 15 min, followed by swirling in fresh acetone and IPA for 30 seconds each and blow-drying with N_2.

The MoS_2/MoS_2 homojunctions (Chapter 3) were assembled via dry transfer by adapting the method described in ref.[57]. Flat polydimethylsiloxane (PDMS) stamps were prepared by mixing Sylgard 184 Silicone Elastomer and Sylgard 184 Curing Agent with a 10:1 weight ratio in a petri dish, followed by degassing and curing in a hand-pumped desiccator at room temperature. Curved PDMS tops were prepared by dropping a small amount of the same mixture onto the flat stamp and curing on a hotplate at 150 °C for 3 hours. Poly(bisphenol A carbonate) (PC) films were prepared on Si/SiO₂ by spin-coating (2000 rpm for 60 seconds) a solution of 5-7 wt.% PC in chloroform, followed by baking at 120 °C for 60 s. The PC was then gently peeled off from the substrate and placed onto the curved-top PDMS stamp. A custom-built transfer stage was used to pick up the top MoS_2 nanosheet with a PDMS/PC stack at a stage temperature of 100 °C for 5-10 minutes. The PDMS/PC/top-MoS_2 stack was then transferred onto the bottom MoS_2 at a stage temperature of 170 °C for at least 10 minutes. The PDMS was then released by gently lifting the

stamp. The homojunction sample was immediately annealed on a hotplate at 200 °C for ~30 s to keep the PC soft, then immediately transferred to a chloroform bath and soaked overnight to remove PC, and annealed in 10^{-6} mbar vacuum at 250 °C (ULVAC MILA-5000) for 8 hours. The SOP for transferring 2D materials can be found: Aligned Transfer SOP.docx.

A standard PMGI/S1813 photolithography process was used to fabricate metal contacts. PMGI SF6 lift-off resist (with a nominal thickness of 280 nm) was spun at 3000 rpm for 45 s and baked at 170 °C for 10 min. S1813 photoresist (with a nominal thickness of 1.3 μm) was then spun at 4000 rpm for 60 s and soft-baked at 115 °C for 1 min. Electrode patterns were directly written with a Heidelberg μPG-501 (Exposure = 20 ms and Defocus = +1 on 285 nm SiO_2/Si) and developed in MF-319 for 35s, followed by rinsing with DI water and blow drying with N_2. Two iterations of photolithography were carried out; 5 nm Cr/50 nm Au contacts were thermally evaporated (Lesker Nano38) to define the probe pads in the first iteration, and then 50 nm Au was evaporated to define contacts connecting the probe pads to the nanosheets in the second iteration. Lift-off was performed in NMP at 60 °C for 1 hr, followed by cleaning in acetone at 40 °C for 10 min, swirling in fresh acetone and IPA for 30 s each, and blow drying with N_2.

The AFM micrographs (Figure 2.14a) show that contacts fabricated by the PMGI/S1813 process exhibit "fences" that are approximately 200 nm tall. These sharp features impede the use of a small lift height during KPFM measurement (Section 2.3.2), as rapid fluctuations in the tip-sample electrostatic interactions can cause instability in the feedback loop. When using a positive photoresist, the side-wall profile is typically coated with metal during evaporation. The metal coating may delaminate, and/or the positive resist may collapse during lift-off, resulting in the formation of "fences" even in the presence of an undercut (Figure 2.14b). In contrast, a negative

resist typically has a natural undercut that minimizes metal coating, resulting in clean lift-off (Figure 2.14c,d). Therefore, we later adopted a lift-off process using a negative resist for device fabrication and patterning ALD films.
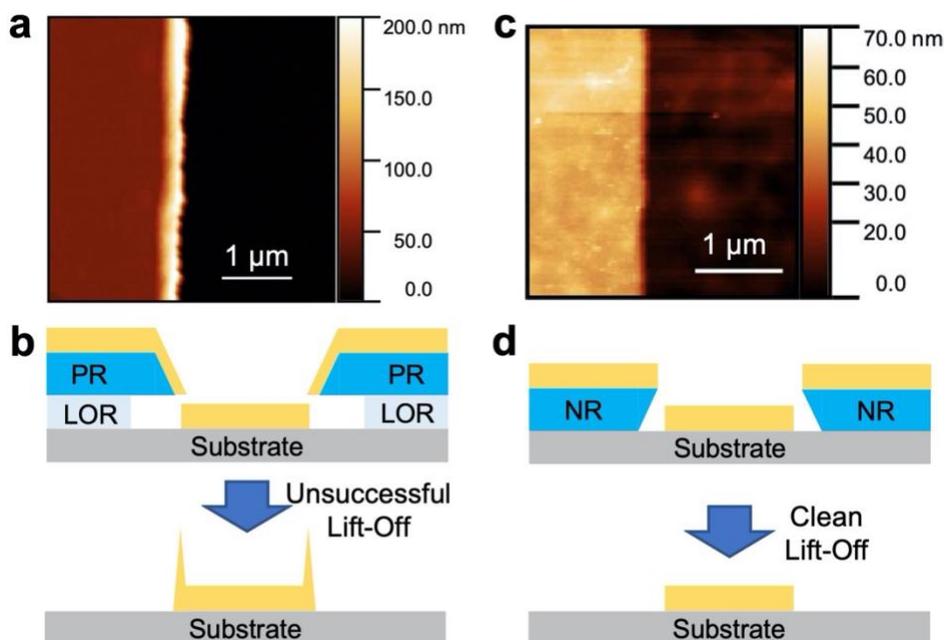
Figure 2.14. Different lift-off results using positive and negative photoresists. (a) AFM and (b) schematic for a bilayer lift-off resist (LOR)/positive resist (PR) process, where "fences" may form. (c) AFM and (d) schematic for a negative resist (NR) process showing clean lift-off.

2.6.2. Fabrication of CVD-MoS$_2$ Electrolyte-Gated Transistors

To test the hypothesis that photoswitchable ion-binding can modulate the electric double-layer capacitance in devices (Chapter 6), CVD-MoS$_2$ electrolyte-gated transistors (EGTs) were fabricated. The monolayer CVD-MoS$_2$ film was synthesized by Stephanie Liu from the Hersam Group at Northwestern University. Several designs of organic EGTs have been proposed[58], where minimizing leakage due to the conducting nature of the electrolyte is a prerequisite. This requires encapsulating the contacts and patterning the semiconducting channel.

To fabricate AlO$_x$-encapsulated contacts, we tested a one-step photolithography and lift-off process using a negative resist, NR74g-1500PY (Futurrex). This negative resist is thermally stable up to 180°C, enabling the patterning of films that require higher growth temperatures. The resist (with a nominal thickness of 1.5 μm) was coated onto sapphire at 3000 rpm for 40 s and baked at 100 °C for 90 s. Electrode patterns were directly written with a Heidelberg μPG-501 (Exposure = 8 ms and Defocus = -1 on sapphire), post-baked at 110 °C for 90 s, and developed in RD-6 for 6-9 s, followed by rinsing with DI water and blow drying with N$_2$. After development, 3 nm Ti and 100 nm Au were evaporated, followed by growing nominally 30 nm AlO$_x$ using ALD at 100°C (Figure 2.15a). The ALD-AlO$_x$ will coat conformally on the exposed surface, encapsulating the whole metal pads (Figure 2.15b). Lift-off was then performed in RR-41 (DMSO) at 80°C for 15 min, followed by a short (3-4 s) sonication at low power (30% power for the sonicator in our lab) to prevent damage to the patterned electrodes.
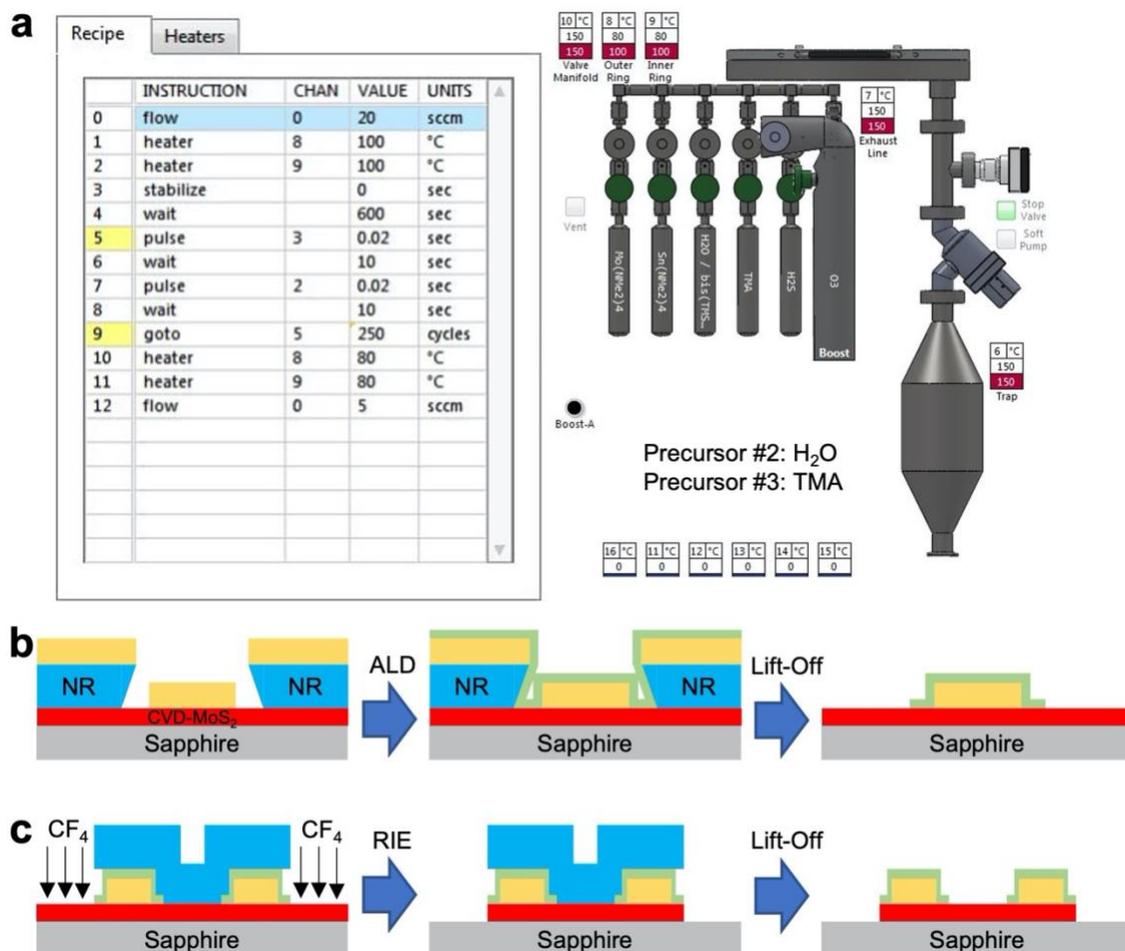
Figure 2.15. Fabrication of CVD-MoS₂ electrolyte-gated transistors (EGTs). (a) ALD growth recipe of nominally 30 nm AlOₓ. Detailed information for the run can be found: 20230227_AluminaDielectric_100C. (b) 1ˢᵗ photolithography and lift-off processes to pattern and encapsulate contacts with ALD-AlOₓ. (c) 2ⁿᵈ series of processes to etch non-channel MoS₂ using reactive ion etching (RIE).

In any of the following situations, dose tests must be conducted at different exposure and defocus conditions to ensure optimal dose:

1. Working with a new substrate: Different substrates produce distinct thin-film interference effects, leading to varying resist exposures.

2. Using resist for the first time in a few months or from a new bottle: Resist can age over time, even when stored in the refrigerator.

3. The laser writer underwent maintenance: The intensity of the UV LED may change.

The pattern used for dose test should include the smallest desirable feature, typically ranging from 2-5 μm. Figure 2.16 shows optical micrographs after development for different exposure and defocus conditions of NR74g-1500PY on sapphire, with a designed feature size of 5 μm. The optimal dose was determined to be exposure = 8 ms and defocus = -1.
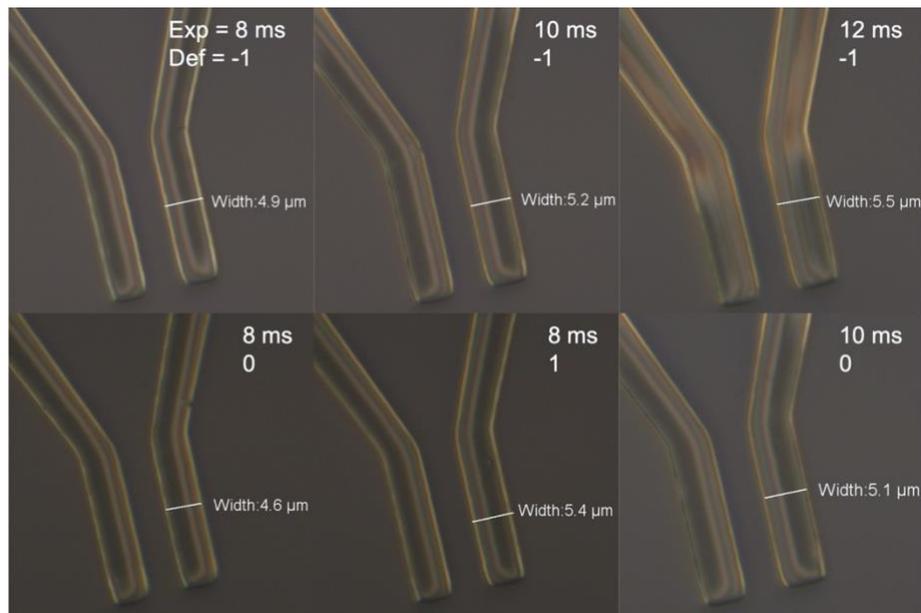
Figure 2.16. Optical micrographs after development for different exposure and defocus conditions of NR74g-1500PY on sapphire. The designed feature size is 5 μm.

We measured the leakage current between the patterned electrodes and the gate electrode (Ag/AgCl) in 10 mM $ZnCl_2$ in acetonitrile and observed a 100× reduction in leakage by encapsulating the contacts (Figure 2.17a,b). To further reduce leakage, the individual channels must be electrically isolated from each other. After AlO_x-encapsulated contacts were patterned on CVD-MoS_2 on sapphire, we used one more step of lithography to protect the MoS_2 channel, exposing the non-channel regions. The unprotected MoS_2 regions were etched for 120 s by oxygen (O_2) plasma (power: 20 W, pressure: 20 mTorr, flow: 50 SCCM), and then by CF_4 plasma (power: 20 W, pressure: 20 mTorr, flow: 50 SCCM) using Samco RIE-10NR (Figure 2.15c),[59] followed by lift-off. The leakage current was reduced by 10× after the exposed MoS_2 was etched (Figure 2.17c,d).
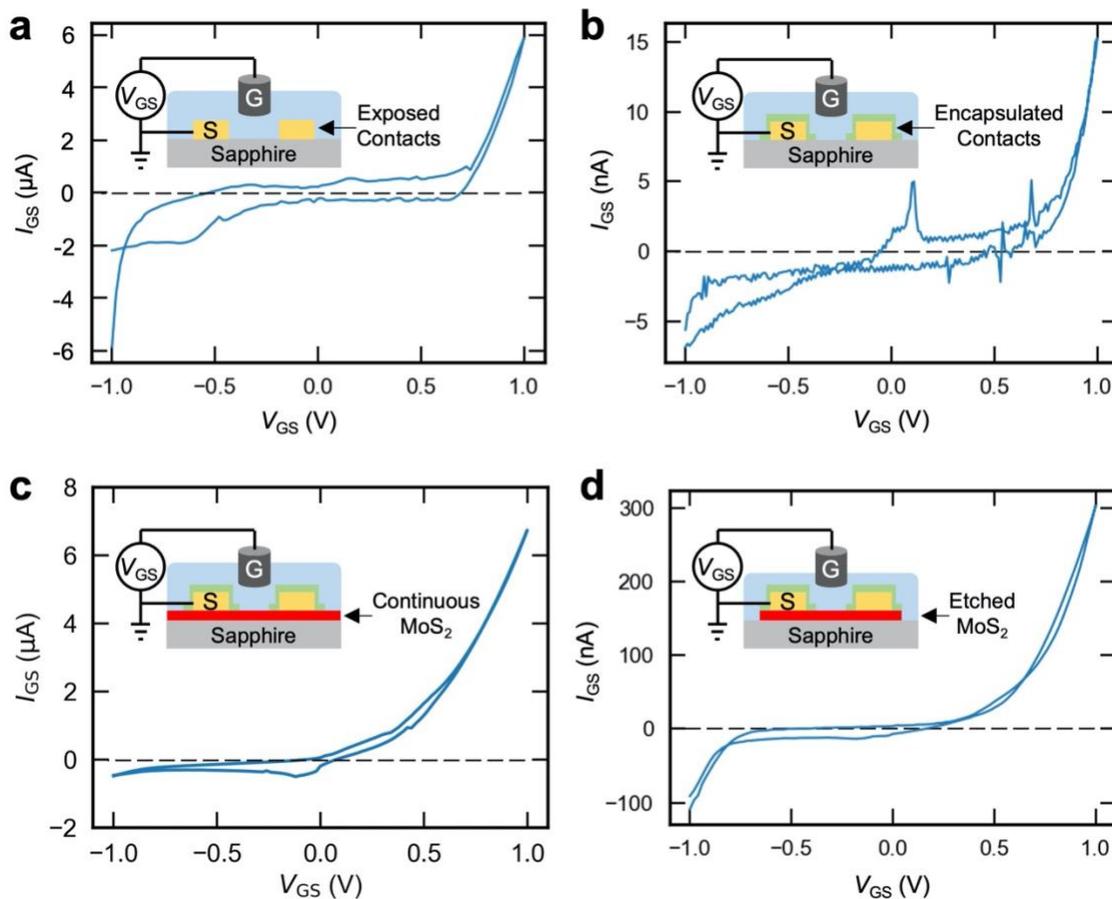
Figure 2.17. Leakage measurements of different process outcomes when fabricating EGTs. Gate-source current I_{GS} vs. gate-source voltage V_{GS} for (a) exposed contacts and (b) AlO$_x$-encapsulated contacts. I_{GS} vs. V_{GS} for (c) continuous MoS$_2$ film and (d) reactive-ion etched, electrically isolated MoS$_2$ film with AlO$_x$-encapsulated contacts.

Figure 2.18 shows the experimental setup for assembling and measuring the EGTs. After two steps of lithography, the device was wire-bonded onto a chip carrier with wires connecting to source meters. A PDMS stamp with a hole was placed on top of the chip as a reservoir for the electrolyte. An Ag/AgCl electrode was immersed into the electrolyte as the gate electrode. A 365 nm UV lamp was used to illuminate the electrolyte that contains photoswitchable molecules.
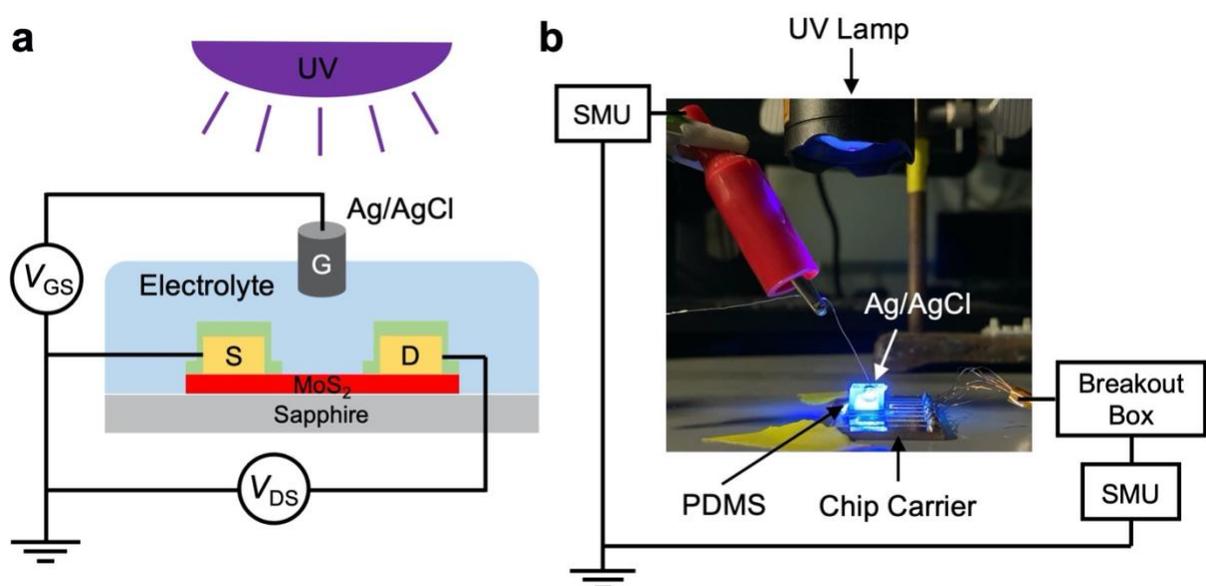
Figure 2.18. EGT assembly and measurement setup. (a) Schematic and (b) actual experimental setups for assembling and measuring EGTs. Keithley 2400 source measure units (SMUs) were used to apply drain-source (V_{DS}) and gate-source (V_{GS}) biases to the devices and to measure the device current.

2.7. Utilization of ChatGPT for Thesis Revision

I adhered to the guidelines provided in ref.[60] concerning the fair use of ChatGPT, an advanced language model developed by OpenAI. Throughout the revision process of this thesis, I employed ChatGPT-4 primarily to improve the grammar, clarity, conciseness, and vocabulary usage of my original writing in Abstract, Section 1.3, Sections 2.3-2.7, Chapters 5-7, and Appendix A. I also used ChatGPT for clarifying concepts such as lock-in amplifiers (Section 2.3), logic-in-memory computing (Section 6.1), photoisomerization (Section 6.2.1), and electric double-layer capacitance (Section 6.3.2), but did not use texts from ChatGPT verbatim.

Examples of prompts I submitted to ChatGPT include requests to revise sentences or paragraphs (Figure 2.19a) and explain concepts (Figure 2.19b). After receiving the output from ChatGPT, I carefully examined and evaluated the suggestions before incorporating them into the thesis. I never used sentences or paragraphs generated by ChatGPT without including my original writing as input, nor did I ask ChatGPT to analyze data or make scientific statements.

a Can you revise: [sentence] or [paragraph]?

Can you revise this: Following the discussion in Chapter 6, leveraging the ion-binding property of certain photoswitches may enable optically modulated memory-in printed TFTs with mixed ionic-electronic transport. A novel device could be printed MoS2 TFTs gated with a photoswitchable (polymeric) ionic liquid. In such a polymer composite, the ionic photoswitch derivatives are attached to the polymer backbone and spatially separated. Photoisomerization may alter the electrostatic interaction between the counterion and the photoswitch, thus changing the counterion mobility and the RC time constant of the composite. Segalman and colleagues synthesized a DAE-based photoswitchable ionic liquid and demonstrated the modulation of anionic conductivity with UV/vis irradiation.14,15 Although the modulation of bulk conductivity still takes tens of minutes, it is possible that the accumulation of ions to the semiconductor by the applied gate electride may accelerate photoswitching at the interface to modualt he EDL capacitance.

Building upon the discussion in Chapter 6, the ion-binding property of specific photoswitches could be harnessed to enable optically modulated memory in printed TFTs featuring mixed ionic-electronic transport. A novel device concept could involve printed MoS2 TFTs gated with a photoswitchable (polymeric) ionic liquid. In such a polymer composite, the ionic photoswitch derivatives would be attached to the polymer backbone and spatially separated. Photoisomerization could alter the electrostatic interaction between the counterion and the photoswitch, thereby changing the counterion mobility and the RC time constant of the composite. Segalman and colleagues synthesized a DAE-based photoswitchable ionic liquid, demonstrating anionic conductivity modulation upon exposure to UV/visible light.14,15 Although the modulation of bulk conductivity currently takes tens of minutes, it is conceivable that the accumulation of ions at the semiconductor surface, driven by an applied gate electric field, could accelerate photoswitching at the interface and modulate the EDL capacitance.

b What is [concept] or [phenomenon]?

What is inside a lock-in amplifier?

A lock-in amplifier is a sophisticated electronic instrument used for extracting weak signals from noisy environments. It works by measuring the amplitude and phase of a signal at a specific reference frequency, effectively filtering out noise that is not at this frequency.

Here's a general overview of the key components you'll find inside a lock-in amplifier:

1. Input stage: The input stage receives the input signal and amplifies it. The input stage may also include filtering options to limit the signal bandwidth before further processing.
2. Reference signal generator: This component generates a reference signal at a specific frequency, which is used to detect the presence of the input signal with the same frequency. The frequency of this reference signal can be adjusted according to the needs of the application.
3. Mixer or multiplier: The mixer (or multiplier) is the core of the lock-in amplifier. It multiplies the amplified input signal with the reference signal, resulting in a product signal that contains the sum and difference frequencies of the two input signals.
4. Low-pass filter: The low-pass filter removes the high-frequency components (sum frequency) from the product signal, leaving only the difference frequency, which is a DC signal proportional to the amplitude of the original input signal at the reference frequency.
5. Phase-sensitive detector: The phase-sensitive detector measures the phase difference between the input signal and the reference signal. This information is essential for determining the phase relationship between the two signals and can be used to reconstruct the original signal.
6. Output stage: The output stage provides the final DC signal, which is proportional to the amplitude of the original input signal at the reference frequency. This output can be further processed or displayed.
7. Control and display: Most modern lock-in amplifiers come with a control panel and display to configure the settings and visualize the output results.

Figure 2.19. Examples of ChatGPT utilization. Representative prompts and transcripts illustrating the use of ChatGPT for (a) revising sentences or paragraphs, and (b) explaining concepts or phenomena.

Chapter 3   Modeling the Performance of Printed vdW TFTs

The following sections have been published in ACS Nano in 2023 by Zhehao Zhu, Joon-Seok Kim, Michael J. Moody, and Lincoln J. Lauhon, and reprinted with permission from American Chemical Society.[1] Zhehao Zhu fabricated the devices and performed the electrical measurements. Zhehao Zhu and Joon-Seok Kim performed the KPFM measurements and analyses. Michael J. Moody wrote the source code for solving the resistor network model. Zhehao Zhu adapted the code and performed the physics-based simulations. Zhehao Zhu and Lincoln J. Lauhon wrote the manuscript. We acknowledge Sonal V. Rangnekar and Professor Mark C. Hersam for the useful discussion on ink processing and printing.

Raw data in this Chapter can be found on the Materials Data Facility (MDF): zhu_transistor.

This Chapter reports experimental investigations of model transistors consisting of 2D nanosheets of controlled thickness that were mechanically exfoliated from bulk crystals and then mechanically transferred to create devices with intersheet junctions (Section 3.1). Kelvin probe force microscopy (KPFM) analysis was used to correlate the channel microstructure with the potential gradient, leading to the discovery that the nanosheet edges, not the intersheet resistance, limit transport due to their impact on charge carrier depletion and scattering (Sections 3.2 and 3.3). The gate-dependent resistor network model introduced in Chapter 2, with experimentally calibrated parameters, is used to establish distinct microstructure-performance relationships created by near-edge and intersheet resistances in printed vdW TFTs (Section 3.4). For a 2D material network consisting of high-mobility and moderately doped nanosheets that produce the near-edge resistance, the optimum nanosheet thickness is dictated by a trade-off between charged

impurity screening and gate screening, and the film mobilities are sensitive to variations in printed nanosheet density (Section 3.5). The model predicts that the removal or passivation of edge states will realize higher film mobilities with thinner nanosheets due to both reduced junction resistances and reduced gate screening. For a network assembled from more defective nanosheets with lower mobility but higher dopant concentration, the model predicts that reducing the nanosheet thickness via development in exfoliation and sorting processes will improve both effective film mobility and on/off ratio.

3.1.   Model System for vdW TFT Performance

The performance of printed MoS_2 transistors varies widely due to variations in thin-film microstructure and the effects of processing on single-sheet mobilities as noted in the Introduction. To illustrate a simple yet quantitative perspective on structure-performance relationships, Figure 3.1a plots previously reported TFT performance characteristics in terms of effective mobility and on/off ratio, with points at the top and to the right indicating higher performance. By coloring the individual data points according to the underlying thin film microstructure (Figure 3.1b), one can observe that channels with nanosheets that are sufficiently large and thin such that they overlap on the basal plane[30] (red points in Figure 3.1a) produce the highest mobility and the largest on/off ratio. Given this microstructure, the maximum mobility is achieved by minimizing the junction resistance between sheets, with the upper bound on the device mobility constrained by the mobility of individual sheets. Practically speaking, some degree of overlap is needed to achieve a sufficiently low junction resistance, which introduces a fundamental performance trade-off: *lowering the junction resistance by increasing the overlap not only increases the on-current, but*

also increases the off-current and may reduce the transconductance due to the increased screening of the bottom gate. Similarly, thick films with multiple layers of overlap will not be optimal due to the introduction of voids (purple points in Figure 3.1a), which do not carry current, increase screening, and may host charged impurities. We therefore conclude that the optimal morphology is that shown in Figure 3.1c. To determine the optimal microstructure of this morphology subject to realistic constraints, we consider a model transistor consisting of two partially overlapping MoS_2 nanosheets (Figure 3.1d). The model system contains each of the performance-limiting interfaces present in an actual printed device with multiple nanosheets, enabling the transistor performance to be accurately modeled as a network of resistors.[61] To establish realistic underlying parameters for the resistor network model, we carried out electrical device measurements and KPFM on devices made from mechanically exfoliated MoS_2. Because state-of-the-art liquid-phase exfoliation processes can produce MoS_2 with single-sheet mobilities approaching that of mechanical exfoliated materials, our model system enables us to identify the microstructure that will maximize the ultimate performance of printed vdW TFTs. Furthermore, we have extended the model to examine how performance trade-offs change when single-sheet mobilities are substantially lower due to unoptimized exfoliation processes.
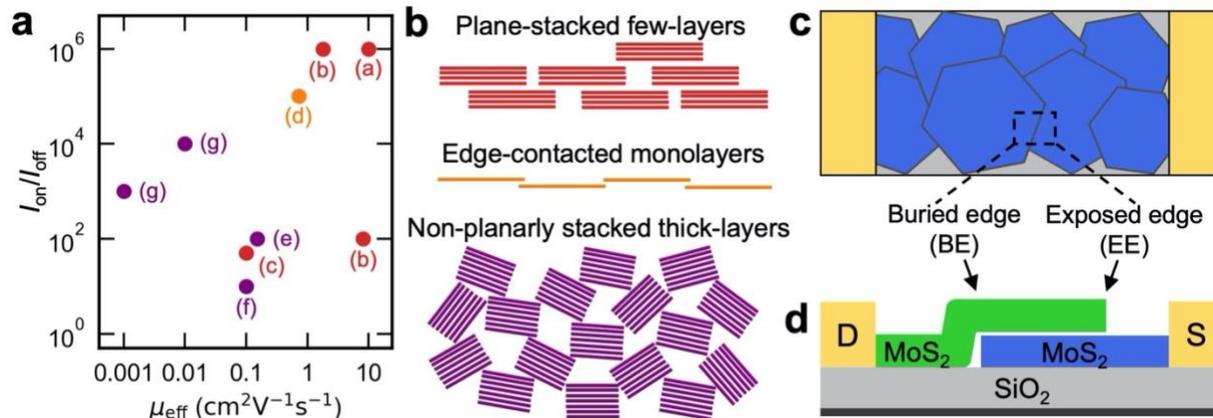
Figure 3.1. Two-nanosheet model system for van der Waals thin-film transistors (vdW TFTs). **(a) On/off ratio I_{on}/I_{off} vs. effective film mobility μ_{eff} for previously reported solution-processed MoS$_2$ TFTs.[15,16,20,26–29] The reference numbers that correspond to the letter labels are listed in Table 3.1. (b) Types of channel cross-sectional microstructures produced by exfoliation and printing. The colors of the schematics are used in (a) to identify the characteristic microstructure associated with the reported device performance. (c) Schematic of a printed vdW TFT with partially overlapping nanosheets. (d) Model transistor consisting of two partially overlapping nanosheets.**

Table 3.1. Corresponding reference numbers for letter labels in Figure 3.1a

Letter label in Figure 3.1a	Corresponding reference number
a	26
b	20
c	29
d	27
e	16
f	15
g	28

Figure 3.2a,b shows a representative 8L/8L homojunction between electrodes 3 and 4; 8L sheets, which are 5.6 nm thick, exhibit bulk-like band structure and permittivity.[45,62] The top 8L (electrodes 1-2) and bottom 8L (electrodes 4-5) devices exhibit typical field-effect transistor (FET) transfer characteristics with on/off ratios I_{on}/I_{off} of 10^5 and peak field-effect mobilities μ_{FE} of 60 $cm^2V^{-1}s^{-1}$ and 36 $cm^2V^{-1}s^{-1}$, respectively. The 8L/8L homojunction device has a reduced I_{on}/I_{off} of 10^4 (Figure 3.2c) and a peak μ_{FE} of 46 $cm^2V^{-1}s^{-1}$ (Figure 3.2d). The lower I_{on}/I_{off} for the 8L/8L is due to the enhanced screening of the gate in the overlap region, which is 16L (11.2 nm) thick. The 8L/8L has a slightly *higher* peak μ_{FE} than the isolated bottom 8L device due to the higher mobility of the constituent top 8L and the lower combined contact resistance, as shown below. At higher gate-source voltages V_{GS}, the μ_{FE} decreases with increasing V_{GS} for all three devices (Figure 3.2d). For the isolated bottom 8L and top 8L devices, the μ_{FE} in strong accumulation (large V_{GS}) is limited by the contact resistance (R_C).[63] The Y-function method[48] (Section 2.2) was used to extract contact resistances of $2R_C = 9.7$ kΩ and $2R_C = 4.3$ kΩ for the bottom 8L and top 8L devices, respectively (Section 3.8.1). The μ_{FE} of the 8L/8L device is impacted by the resistances of contacts 3 and 4 and the junction resistance R_J.[64] Assuming that the contact resistance of the 8L/8L device is an average of the contact resistances in the single-sheet devices, the Y-function method identifies an additional series resistance of 12.3 kΩ in strong accumulation (Section 3.8.1), which we attribute to R_J. However, we note that the junction region extends over several microns. To understand the behavior of printed 2D devices with overlapping flakes, we need to understand how the potential varies across the junction region as the relative magnitudes of the sheet resistance and intersheet resistance change with gate voltage.
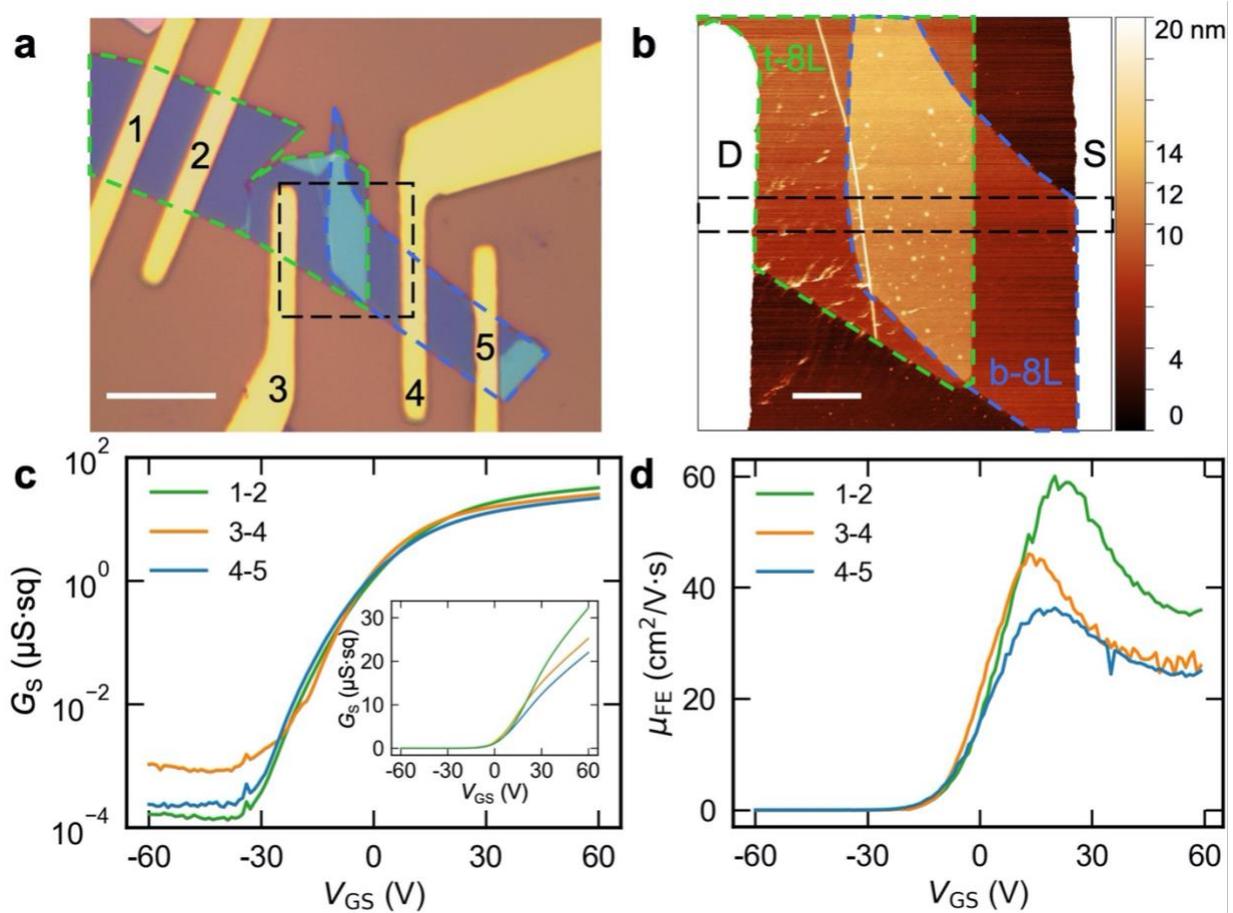
Figure 3.2. Surface topography and field-effect characteristics of 8L/8L homojunction device. (a) Optical micrograph of an 8L-MoS$_2$/8L-MoS$_2$ homojunction device. Electrodes 1-2 and 4-5 define single-sheet MoS$_2$ FETs, while electrodes 3-4 define the 8L/8L homojunction FET. The scale bar is 10 μm. (b) Atomic force micrograph (AFM) of the region indicated by a black dashed square in (a). The scale bar is 2 μm. Green dashed line indicates the top 8L (t-8L) sheet, while blue indicates bottom 8L (b-8L) sheet. (c) Effective sheet conductance $G_S = (I_{DS}/V_{DS})(L/W)$ vs. gate-source voltage V_{GS} and (d) field-effect mobility $\mu_{FE} = (dI_{DS}/dV_{GS})(L/V_{DS}WC_{ox})$ vs. V_{GS}, where C_{ox} is the capacitance of 285 nm SiO$_2$, for the devices shown in (a) at drain-source voltage $V_{DS} = 0.5$ V.

3.2. Identification of Limiting Resistance in 8L/8L Homojunction Device

To characterize the evolution of the junction resistance with bias, and thus quantify the impact on mobility, KPFM (Sections 2.3 and 3.8.2) was used to measure spatially resolved surface potential profiles of a representative region (Figure 3.3a) in both moderate accumulation ($V_{GS} = 0$ V) and depletion ($V_{GS} = -15$ and -45 V) based on the transfer curve in Figure 3.2c. Assuming that the current density is uniform across the width of the channel, the potential drop along the channel is given by $dV/dx = J\rho$, where J is the current density and ρ is the resistivity. Hence, regions of rapid potential drop are associated with a large resistivity. When the homojunction device is biased to moderate accumulation at $V_{GS} = 0$ V and $V_{DS} = 1$ V, potential drops corresponding to resistances of 2.9 MΩ, 0.6 MΩ, and 0.5 MΩ, and 0.3 MΩ were measured at the homojunction region, source, drain, and the channel outside of the junction (*i.e.*, two single-sheet regions), respectively (Figure 3.3b, $V_{DS} = -1$ V data in Figure 3.1b). Consistent with the Y-function analysis, the junction resistance dominates the overall resistance in the on-state, confirming that μ_{FE} for the 8L/8L device is limited by the junction. Specifically, the junction resistance is ~10× larger than the combined resistance of the single-sheet regions, confirming that the on-state conductance of a network consisting of such nanosheets will be limited by the junction resistance rather than the single-sheet resistance.[30,65] (We note that the junction and contact resistances determined by the KPFM potential drop are slightly higher than that extracted from the transfer curves because the KPFM analysis was conducted at $V_{GS} = 0$ V to keep the current density low and minimize the potential for device degradation during the measurement). Given the out-of-plane Debye length of 4.4 nm (Section 2.1),[45] the surface potential in the overlap region is primarily determined by the top-8L (5.6 nm) sheet, which screens the bottom-8L sheet. Since little potential drop is observed along

the overlap region, and the potential drops abruptly where the top sheet overlaps the buried edge of the bottom sheet (0.67 V), we conclude that a substantial fraction of the current is forced from the top sheet into the bottom sheet in the vicinity of the buried edge (BE) due to a local region of high resistivity.

The higher local resistivity near the buried edge may arise from an increase in scattering or reduction in carrier concentration, both of which could result from trapped charges.[37] Indeed, the surface potential in equilibrium at $V_{DS} = 0$ V exhibits a 50 mV peak near the buried edge (Figure 3.3c), consistent with the presence of fixed negative charges at the buried edge and/or depletion of the top sheet above the buried edge caused by the trapped charges. We therefore attribute the large near-edge resistivity to the impact of charged impurities at the buried edge on carrier scattering and depletion in the top sheet.[66] Oxidation of the buried edge, which is expected under ambient conditions,[67–70] is also expected to cause local carrier depletion in the bottom sheet.[41,70,71] For completeness, we note that phonon scattering may be enhanced by current crowding near the buried edge,[39] but contribution is estimated to be negligible (Section 2.1.3). We also note that tensile and compressive strains present in the top nanosheet where it overlaps the buried edge may modify the MoS_2 band gap and increase the local conductivity.[72,73] If strain has a larger impact on the local charge transport than charged impurities, there would be a negligible potential drop. Hence, the charged impurities must play a dominant role in the observed potential drop and the large near-edge resistivity. Although the KPFM in Figure 3.3c also suggests the presence of negative charges trapped at the exposed edge of the top sheet, the potential drop under bias is relatively small in this region because the trapped charges are more effectively screened. In moderate accumulation ($V_{GS} = 0$ V), the high carrier concentration in the bottom sheet effectively

screens the charged impurities at the exposed edge of the top sheet, reducing the impact on the bottom sheet resistivity. As the device moves into depletion (V_{GS} = -15 V and -45 V in Figure 3.3b, Figure 3.2c), the carrier concentration in the bottom sheet decreases, leading to an increased potential drop below the exposed edge (due to reduced screening) and a larger potential gradient in the bottom sheet region. Considering the differential impact of trapped charges on the upper and lower sheets in homojunctions, it is clear that the general performance limits of printed TFTs are not determined solely by the interfacial resistance between basal planes (*i.e.*, intersheet resistance).[16,26,28,30,74] Furthermore, the observed near-edge resistance creates distinct trade-offs when optimizing the microstructure for printed vdW TFTs, as shown below.
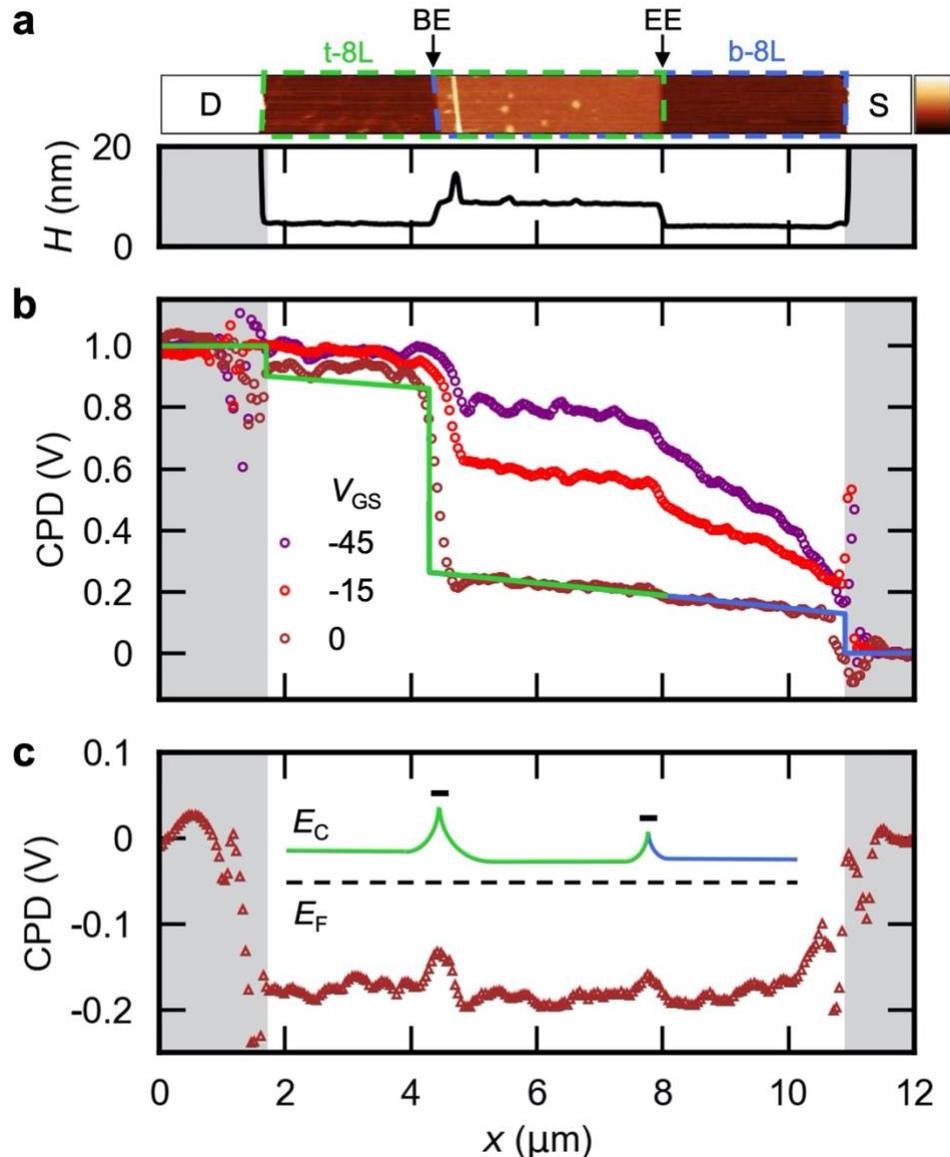
Figure 3.3. Kelvin probe force microscopy (KPFM) analysis of surface potential variations in biased 8L/8L device. (a) AFM topography (color scale = 0 – 20 nm) of a representative region in the 8L/8L device, as indicated by a black dashed square in Figure 3.2b. H **shows the height profile in this region. (b) Measured (open circles) and simulated (lines) contact potential difference (CPD) profiles for region shown in (a) at** $V_{DS} = 1$ **V. For each** V_{GS}**, the CPD under** $V_{DS} = 0$ **V was subtracted from the CPD under** $V_{DS} = 1$ **V.[43,53] The parameters used to generate the fit are provided in Table 3.2. (c) CPD at** $V_{DS} = 0$ **V and** $V_{GS} = 0$ **V. Each CPD profile measured by KPFM was offset by setting the potential at grounded source to zero.**

3.3. Influence of Nanosheet Thickness on Limiting Resistance

We analyzed additional homojunction devices of varied sheet thicknesses to confirm the influence of sheet edges on local resistivity and to provide experimental constraints on a resistor network model of the homojunction device. Broadly speaking, we hypothesize that reduced screening in thinner sheets[38,45] (less than the Debye length, see Section 2.1) will lead to larger potential drops at sheet edges, as was observed in the thicker 8L/8L device when gated into depletion. To test this hypothesis, asymmetric 5L/1L and symmetric 1L/1L devices were characterized (Figure 3.4, Figure 3.12, Figure 3.13, and Figure 3.14) using the approach demonstrated above for the 8L/8L device. Because the threshold voltages vary between devices due to variations in intrinsic doping and screening of interfacial charges, the transfer curves in Figure 3.12d and Figure 3.13d were used to identify gate voltages that produce equivalent degrees of accumulation and depletion for KPFM analysis in Figure 3.4b,d (accumulation data) and Figure 3.14 (data in accumulation and depletion). When the 5L/1L device is in accumulation ($V_{GS} = 20$ V), the transistor shows an abrupt potential drop of 0.8 V near the exposed edge but a negligible potential drop near the buried edge (Figure 3.4b), unlike the 8L/8L device. We propose that the trapped charges at the buried 1L edge are more effectively screened by the top 5L sheet than the trapped charges in the exposed 5L edge are screened by the bottom 1L sheet, leading to a highly resistive region in the 1L at the exposed edge. KPFM analysis of the 1L/1L device supports the claim that variations in screening of trapped charge influence the magnitude of potential drops at edges; comparable potential drops are observed at the buried (0.23 V) and exposed edges (0.19 V)

(Figure 3.4d) in accumulation (V_{GS} = 30 V), indicating that the top and bottom sheets are similarly impacted by localized negative charges that are incompletely screened. The slightly larger potential drop near the buried edge is likely due to the lower carrier concentration in the top 1L at the junction, which reduces the free-carrier screening. The largest local potential drop (0.60 V) in the 1L/1L device appears to be associated with a 1.5 nm wrinkle (Figure 3.4d and full AFM in Figure 3.13b) that was formed during the transfer process.[75] Interestingly, a similar size wrinkle in the top 8L sheet of the 8L/8L device has a negligible impact on the potential (Figure 3.3a,b), potentially due to more effective screening. Another source of potential drop, not present in the 8L/8L homojunction, is the band offset between the sheets; the larger work function of the top 5L may further deplete the 1L sheet (Figure 2.7).
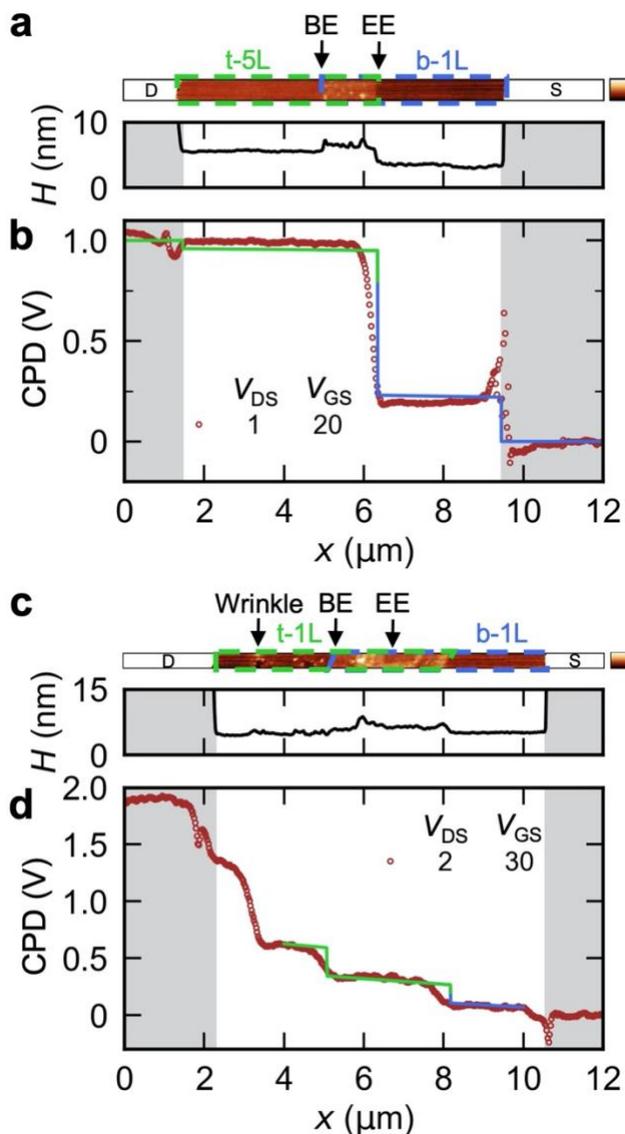
Figure 3.4. Influence of nanosheet thickness on potential drops in accumulation. AFM topography and height (*H*) profiles of representative regions in the (a) 5L/1L and (c) 1L/1L devices, respectively. Scale bar = 0 – 10 nm. (b) and (d) Measured (open circles) and simulated (solid lines) CPD profiles for the (b) 5L/1L at V_{DS} = 1 V and V_{GS} = 20 V, and (d) 1L/1L at V_{DS} = 2 V and V_{GS} = 30 V, representing equivalent degrees of accumulation Green represents the top sheet, while blue represents the bottom sheet. The parameters used to generate the fits are provided in Table 3.2.

3.4. Extraction of Near-Edge Resistivity Ratio in Model Transistors

Figure 3.5a presents a gate-dependent resistor network model that we developed to test our interpretation of the KPFM data and predict the optimal microstructure for printed TFTs. The assumptions are described in the paragraph below and additional details are provided in Section 2.1. The model is based on a transmission line model for partially overlapping channels[39] and incorporates spatially varying resistivities, influenced by gate screening,[40] and trapped charges at the edges of sheets.[28,36,41] The horizontal resistors represent the ohmic conduction associated with intrasheet (in-plane) band-like transport in accumulation,[37] which has been shown to dominate the overall charge transport in printed MoS_2 network at sufficiently high gate voltages.[42] The vertical resistors represent the effective resistance considering the anisotropic resistivity[44] and the mobile carrier concentration, which depends on the applied gate voltage (Section 2.1). We note that our interpretation of the near-edge resistance is insensitive to the details of the intersheet transport model; if intersheet processes limit the transport at the junction, the potential would drop along the overlap region rather than locally near the nanosheet edges. We account for gate screening by using Thomas-Fermi charge screening theory to estimate the carrier concentration in each monolayer as a function of distance from the dielectric interface.[40] We reduce the number of independent variables by treating the junction resistance R_J as a function of two independent variables, the near-edge sheet resistance ratio $R_{S,E}/R_S$ and the intersheet resistivity ratio $\rho_{i,E}/\rho_i$. $R_{S,E}/R_S > 1$ and/or $\rho_{i,E}/\rho_i > 1$ represent conditions under which the near-edge resistivities are greater than those in the middle of the homojunction (Figure 3.5a) due to unscreened charged impurities identified in KPFM analysis. The effective edge lengths, *i.e.*, the size of the regions depleted by trapped charges, were estimated for each thickness by analyzing the 2D and 3D Debye lengths

(Section 2.1 Figure 2.2).[38] For the 8L/8L homojunction, KPFM analysis indicated that the bottom 8L resistivity is only weakly perturbed at the location of the exposed top 8L edge (*i.e.*, $R_{B,EE}/R_B = 1$). Details for calculating resistances, assigning effective edge lengths and near-edge resistivity ratios, and solving the network are provided in Section 2.1.

We empirically determine the possible range of the sheet resistance ratio $R_{S,E}/R_S$ and intersheet resistivity ratio $\rho_{i,E}/\rho_i$ in our model transistors by using the measured junction resistances and potential profiles as constraints in the resistor network model (Figure 3.5 and Section 3.8.4). Figure 3.5b shows that although the measured junction resistance is consistent with a range of sheet resistance and intersheet resistivity ratios, it is clear that the sheet resistance at the sheet edges is at least ~1000 larger than that in the middle of the junction (*i.e.*, $R_{S,E}/R_S > 1000$), validating our qualitative explanation of the KPFM data. For the 8L/8L homojunction, equivalently good fits of the junction resistance R_J are produced with near-edge sheet resistance ratio $R_{S,E}/R_S$ between 2000 and 5000 as the near-edge intersheet resistivity ratio $\rho_{i,E}/\rho_i$ adopts values ranging from 1 to 1000 (Figure 3.5b). (The simulated R_J is insensitive to $\rho_{i,E}/\rho_i$ for $\rho_{i,E}/\rho_i > 100$ because the intersheet resistance depends on the inverse of ρ_i due to parallel conduction pathways.) The best fit is given by $R_{S,E}/R_S = 3500$ and $\rho_{i,E}/\rho_i = 10$ as shown in Figure 3.5c. Despite the large variation in $\rho_{i,E}/\rho_i$, the possible values for $R_{S,E}/R_S$ are well constrained, indicating that the dominant factor for the junction resistance is the near-edge sheet resistance of the top sheet where it overlaps with the buried edge (Figure 3.16). When the model includes gate screening but not enhanced near-edge resistivity ratios (*i.e.*, $R_{S,E}/R_S = \rho_{i,E}/\rho_i = 1$), it cannot reproduce the measured junction resistance (Figure 3.5b) and potential drop (Figure 3.5c); an abrupt potential drop near the buried edge is observed only when $R_{S,E}/R_S \gg 1$.
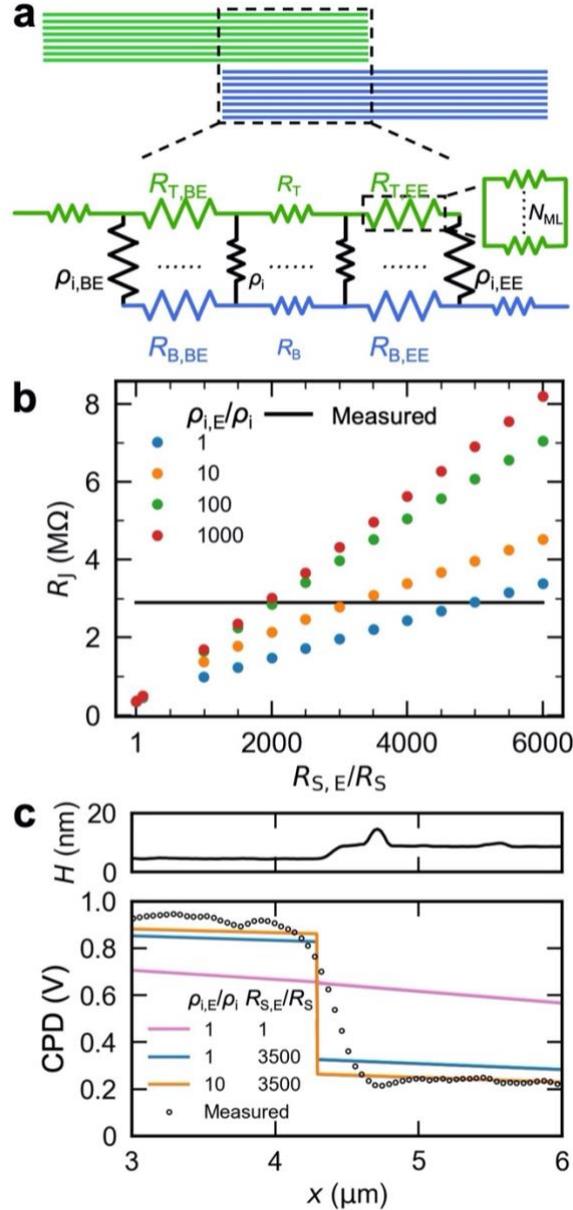
Figure 3.5. Extraction of near-edge resistivity ratios in model transistors. (a) Resistor network model that reproduces the on-state characteristics of a two-nanosheet device with trapped charges at edges. R_T and R_B represent the gate-dependent sheet resistances of the top and bottom nanosheets, respectively. Each nanosheet was modeled as N_{ML} parallel resistors. ρ_i represents the specific intersheet resistivity. The near-edge resistivities are greater than those in the middle of the junction. Sensitivity of **(b)** junction resistance R_J and **(c)** CPD to the near-edge sheet resistance ratio $R_{S,E}/R_S = R_{T,BE}/R_T = R_{B,BE}/R_B = R_{T,EE}/R_T$ and intersheet resistivity ratio $\rho_{i,E}/\rho_i = \rho_{i,BE}/\rho_i = \rho_{i,EE}/\rho_i$ for the 8L/8L device. Note that $R_{B,EE}/R_B = 1$ for the 8L/8L device.

The resistor network model reproduces the 5L/1L (Figure 3.4b) and 1L/1L (Figure 3.4d) KPFM data as well, supporting our claim that the dominant resistance is determined by the thickness-dependent free-carrier screening of trapped charges. The potential profile for the 1L/1L was reproduced with an average $R_{S,E}/R_S = 500$ at both edges (Figure 3.4d and Figure 3.6a,b), confirming that the near-edge sheet resistances are increased by the weak screening of charged impurities. Interestingly, an average $R_{S,E}/R_S$ of 50,000 is necessary to reproduce the observed potential drop in the 5L/1L device (Figure 3.4b and Figure 3.6c,d). As discussed above, the bottom 1L sheet is further depleted due to charge transfer to the narrower gap top 5L sheet, further reducing the screening of charged impurities and increasing the bottom 1L sheet resistance where it overlaps with the exposed top 5L edge. This observation is in consistent with a previous study reporting that a large work function difference between sheets results in a large junction resistance.[64]
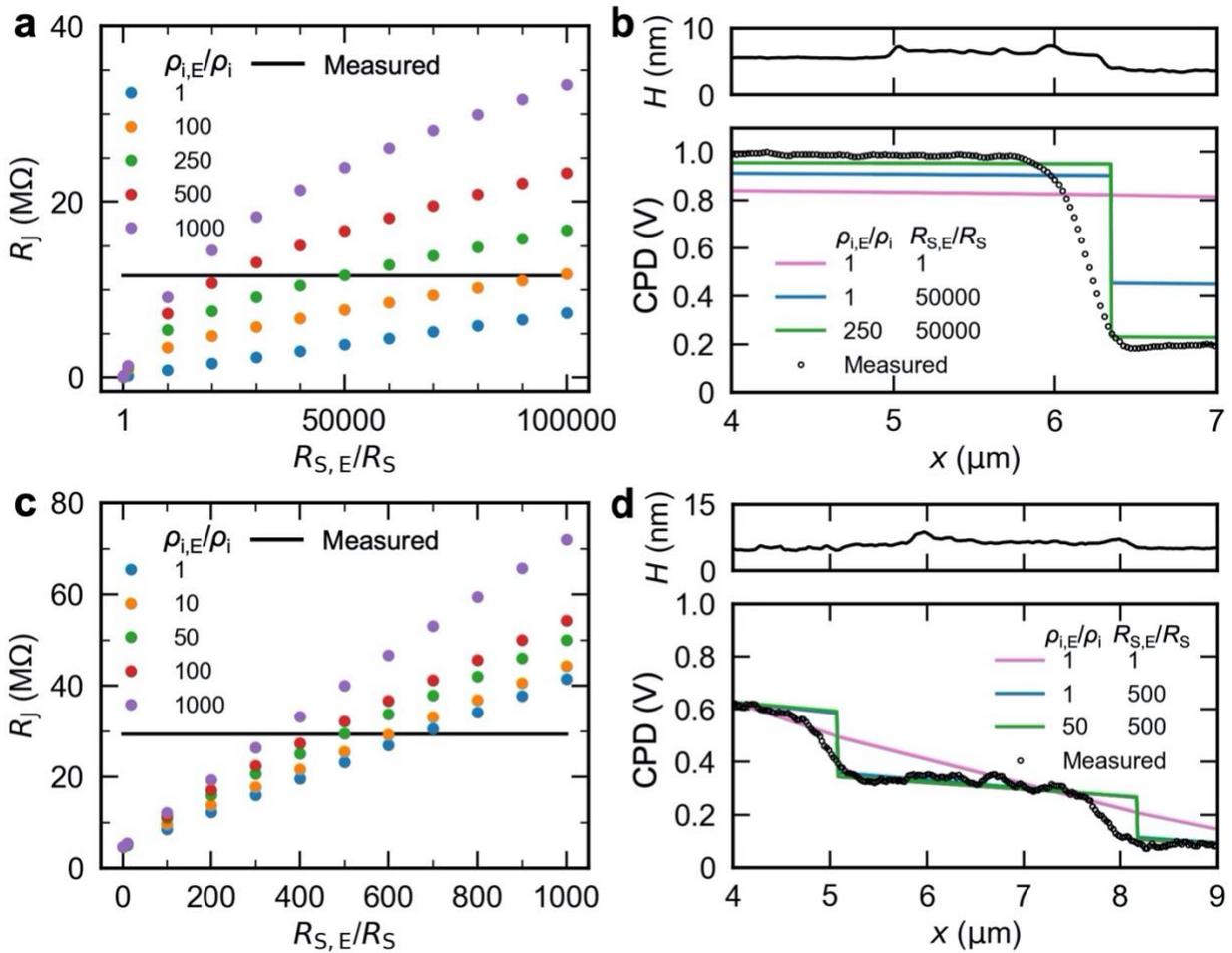
Figure 3.6. Parameter sensitivity analyses of the model for the 1L/1L and 5L/1L devices. Sensitivity of (a) R_J and (b) CPD to sheet resistance ratio $R_{S,E}/R_S = R_{T,BE}/R_T = R_{T,EE}/R_T = R_{B,BE}/R_B = R_{B,EE}/R_B$ and intersheet resistivity ratio $\rho_{i,E}/\rho_i$ for the 1L/1L. We note that when $R_{S,E}/R_S$ becomes large enough, $\rho_{i,E}/\rho_i$ makes a very small difference in R_J and surface potential, hence the simulations for $\rho_{i,E}/\rho_i$ of 1 and 50 overlap in (b). Sensitivity of (c) R_J and (d) CPD to sheet resistance ratio $R_{S,E}/R_S = R_{T,EE}/R_T = R_{B,BE}/R_B = R_{B,EE}/R_B$ and intersheet resistivity ratio $\rho_{i,E}/\rho_i$ for the 5L/1L. Note that $R_{T,BE}/R_T = 1$ for the 5L/1L device.

Table 3.2. Parameters used to generate fits for the potential profiles of fabricated homojunction devices.

Resistivity ratio	8L/8L (Figure 3.3b)	5L/1L (Figure 3.4b)	1L/1L (Figure 3.4d)
$R_{B,BE}/R_B$	3500	50000	500
$R_{T,BE}/R_T$	3500	1	500
$\rho_{i,BE}/\rho_i$	10	250	50
$R_{B,EE}/R_B$	1	50000	500
$R_{T,EE}/R_T$	3500	50000	500
$\rho_{i,EE}/\rho_i$	10	250	50

3.5.   Distinct Trade-Offs When Optimizing Microstructure of Printed vdW TFTs

The combined KPFM and resistor network analysis demonstrates that the effective mobility and on-state conductance of devices incorporating partially overlapping nanosheets may be limited by the increased resistance at nanosheet edges rather than the intersheet resistance. We next use the model (details in Section 2.1) to identify the optimum printed film microstructure as a function of the nanosheet dimensions, which are determined by exfoliation and sorting processes, and the nanosheet stacking morphology, which is determined by the printing process. We consider a printed film morphology with low porosity (Figure 2.3), where the nanosheets are sufficiently large and thin to form conformal junctions,[30] as has been experimentally demonstrated in ref.[29] via inkjet printing and in ref.[76] via aero-jet printing. Figure 3.7 shows the result of simulations a device with a 10 μm channel with varying nanosheet thickness, total film thickness, and nanosheet density. A typical dopant concentration of 10^{18} cm^{-3} was assumed to determine the screening lengths (Table 2.1).[43] Intersheet-resistance-limited devices, a scenario that is commonly assumed in the literature,

are modeled by assuming that the intrasheet and intersheet resistances do not vary along the channel, *i.e.*, $R_{S,E}/R_S = \rho_{i,E}/\rho_i = 1$. Edge-resistance-limited devices are modeled by assuming that the intrasheet resistances are much larger at sheet edges, while the intersheet resistances do not vary, *i.e.*, $R_{S,E}/R_S \gg 1$ and $\rho_{i,E}/\rho_i = 1$. Significantly, we find that edge-resistance-limited devices exhibit fundamentally different trade-offs between microstructure and performance compared to the intersheet-resistance-limited devices.

We first examine how mobility varies with film thickness (the number of stacked nanosheets) by using fixed single-sheet dimensions (6L thick, 700 nm diameter) and densities that have been achieved by electrochemical exfoliation (Figure 3.7a).[26] The single-sheet mobility of 50 cm^{2}V^{-1}s^{-1}, which has been demonstrated for individual nanosheets isolated from inks,[16] is held constant to identify film thicknesses and near-edge resistances that achieve a target effective mobility of 10 cm^{2}V^{-1}s^{-1} (ref.[9]). (Smaller single sheet mobilities are considered below). In all cases, the effective mobility increases monotonically with decreasing thickness because the gate screening decreases (Figure 3.7a, right to left). If the near-edge resistance is negligible ($R_{S,E}/R_S = 1$, dot-dashed line in Figure 3.7a), the printed film thickness must be less than 5 stacked nanosheets to achieve the target mobility of 10 cm^{2}V^{-1}s^{-1}. If near-edge resistance is significant, even thinner films must be targeted. Hence, we find that edge passivation relaxes constraints on the printing process. Although percolative networks have been formed from as few as two nanosheet stacks (layers of nanosheets) via self-assembly at liquid/liquid interface,[27] films prepared by top-down deposition methods (*e.g.*, spin-coating) typically require at least three nanosheet stacks to achieve percolation.[20,26] Therefore, the simulations below focus on experimentally achievable microstructures in which nanosheets are 6L thick and films are 3 nanosheets thick.
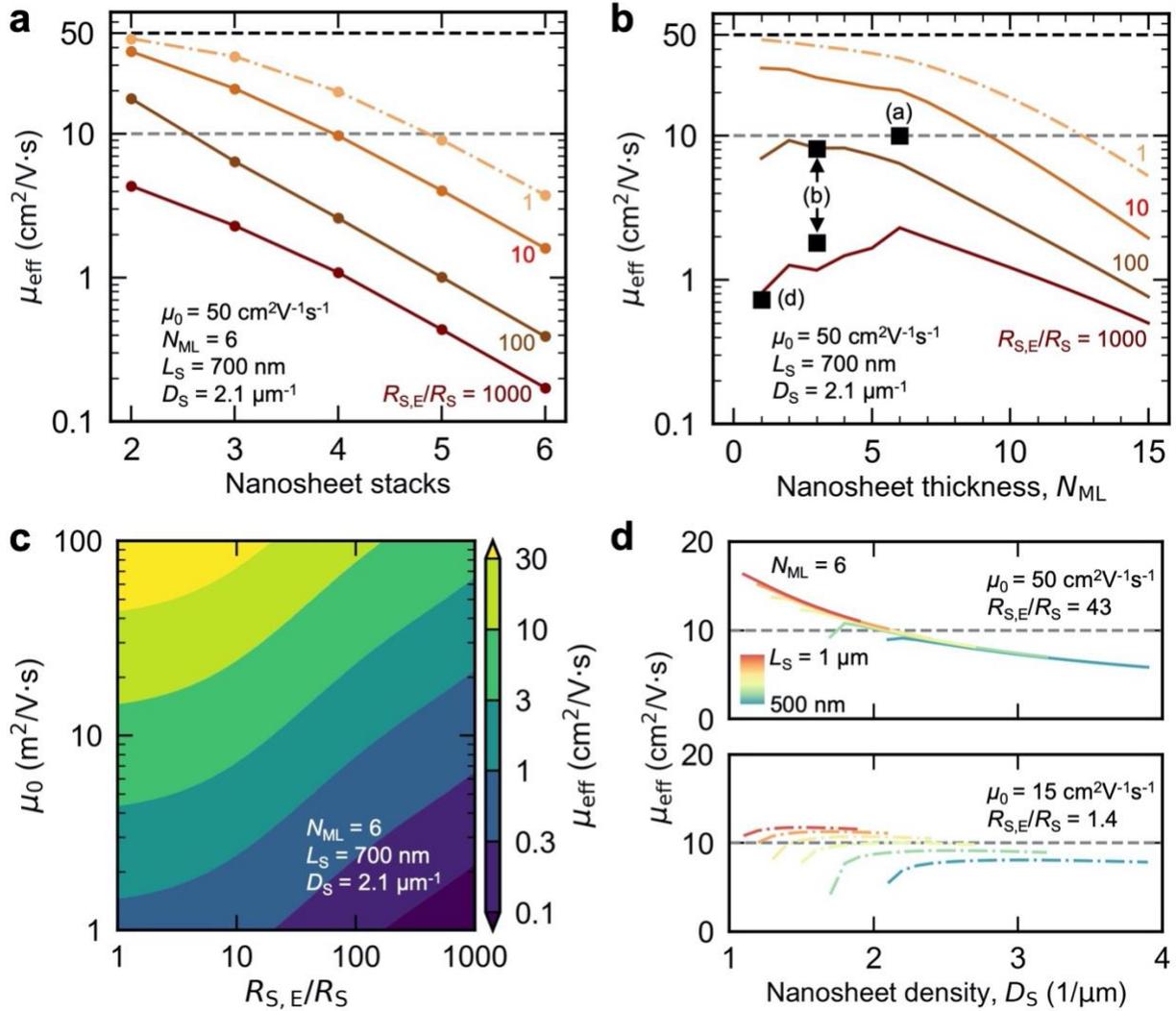
Figure 3.7. Pathways to optimizing printed vdW TFTs. Simulated effective mobility μ_{eff} vs. (a) number of stacked nanosheets, (b) nanosheet thickness N_{ML} (number of monolayers per nanosheet), and (c) single-sheet mobility μ_0 and $R_{S,E}/R_S$ at the median density $D_S = 2.1\ \mu m^{-1}$ (number of nanosheets per channel length) for nanosheet size $L_S = 700$ nm. The black squares in (b) represent the μ_{eff} in refs.[20,26,27] vs. the reported average N_{ML}. The reference numbers corresponding to the letter labels are listed in Table 3.1. (d) μ_{eff} vs. D_S (color scale: $L_S = 500$ nm-1 μm) for $\mu_0 = 50\ cm^2V^{-1}s^{-1}$ and $R_{S,E}/R_S = 43$ (top) and $\mu_0 = 15\ cm^2V^{-1}s^{-1}$ and $R_{S,E}/R_S = 1.4$ (bottom), both of which are on the $\mu_{eff} = 10\ cm^2V^{-1}s^{-1}$ contour line in (c). In (a) and (b), the dot-dashed lines represent $R_{S,E}/R_S = 1$ (i.e., interface-resistance-limited regime), while the solid lines represent $R_{S,E}/R_S = 10$-1000 (i.e., edge-resistance-limited regime); $\mu_0 = 50\ cm^2V^{-1}s^{-1}$. In (a), (c), and (d), $N_{ML} = 6$. In (b)-(d), the number of stacked nanosheets is 3. In all subfigures, the dopant concentration is $10^{18}\ cm^{-3}$, $\rho_{i,E}/\rho_i = 1$, and the channel length is 10 μm.

As a base case, we first consider devices limited by intersheet resistance (Figure 3.7b dot-dashed line) and observe that the effective mobility increases monotonically with decreasing thickness as the gate screening decreases, approaching the single-sheet limit of 50 cm^{2}V^{-1}s^{-1}. The target effective mobility of 10 cm^{2}V^{-1}s^{-1} is met for sheet thicknesses less than 12L; if the average lateral size is increased to 1.2 μm, the target mobility is achieved over sheet thicknesses from 1L to 15L (Figure 3.8a). In this scenario, liquid phase exfoliation and sorting processes should target the production of large diameter nanosheets while keeping thicknesses greater than the Debye length (e.g., $N_{ML} \geq 6L$ for MoS$_2$) so that the junction resistance arising from work function differences between sheets is minimized. Efforts to reducing the sheet thickness below 6L will produce only modest improvements in effective mobility.

The dependence of effective mobility on sheet thickness changes when transport is limited by the near-edge resistance, as shown by simulations with $R_{S,E}/R_S = 1000$ (Figure 3.7b and Figure 3.8a), which is comparable to the value ($R_{S,E}/R_S = 3500$) extracted in KPFM analysis. There is now an optimum sheet thickness of 6L, regardless of sheet size (Figure 3.7b and Figure 3.8a), that arises from a trade-off between gate and charged impurity screening. Although making the sheets thinner reduces gate screening, charged impurity screening is also weakened, dramatically increasing the resistance near the nanosheet edges. When nanosheet thicknesses increase beyond the optimal 6L (peak in dark red curve in Figure 3.7b, Figure 3.8, Table 2.2), the effective mobility decreases due to increasing gate screening *and* increasing near-edge resistance (the trapped charge density increases linearly with flake thickness). In this scenario, the only route to achieve the target effective mobility for typical sheet sizes (*i.e.*, $L_S < 1$ μm) is to develop processing procedures that

reduce the concentration of trapped charges at edges. As a concrete example, if the near-edge sheet resistance is reduced 100-fold compared to that of our current devices (*i.e.*, $R_{S,E}/R_S$ is reduced from ~1000 to ~10), films with nanosheets that less than 9L thick should be able to meet the target mobility of 10 $cm^2V^{-1}s^{-1}$. Edge passivation will also reduce variations in mobility for sheet thickness < 6L (Figure 3.7a, $R_{S,E}/R_S$ = 1-100).
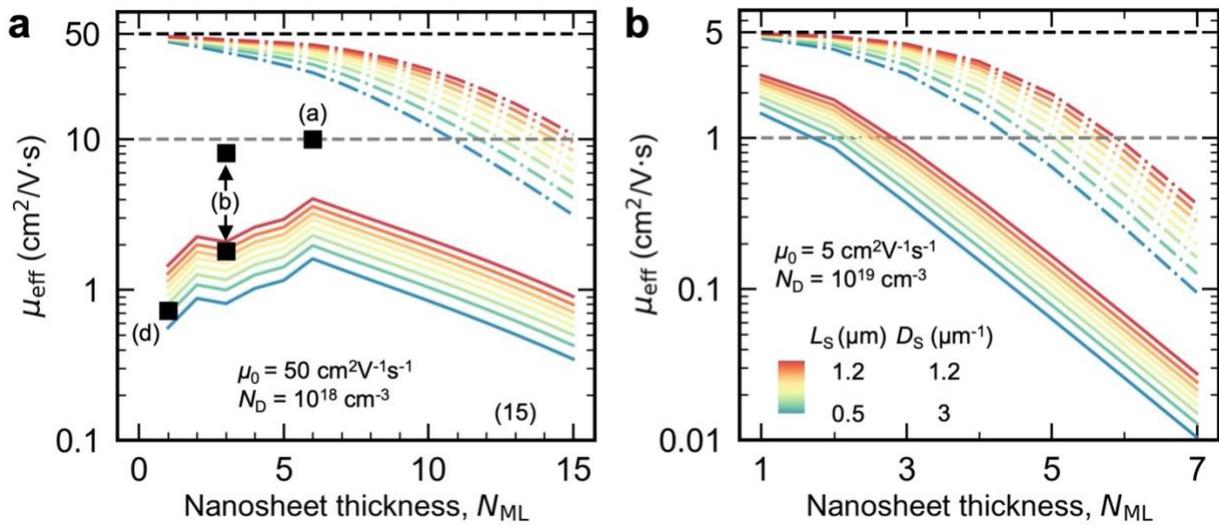
Figure 3.8. Nanosheet thickness-dependent simulation results for printed vdW TFT with different single-sheet mobilities and dopant concentrations. $\mu_{eff,med}$ **vs.** N_{ML} **at the median density** D_S **= 3-1.2 μm^{-1} for** L_S **= 500 nm-1.2 μm. In (a),** μ_0 **is 50 $cm^2V^{-1}s^{-1}$ and** N_D **is 10^{18} cm^{-3}. In (b),** μ_0 **is 5 $cm^2V^{-1}s^{-1}$ and** N_D **is 10^{19} cm^{-3}. The dot-dashed lines represent** $R_{S,E}/R_S = \rho_{i,E}/\rho_i =$ **1 (*i.e.*, interface-resistance-limited regime), while the solid lines represent (a)** $R_{S,E}/R_S$ **= 1000 and (b)** $R_{S,E}/R_S$ **= 100 with** $\rho_{i,E}/\rho_i$ **= 1 (*i.e.*, edge-resistance-limited regime). The number of stacked nanosheets is 3. The channel length is 10 μm. The reference numbers that correspond to the letter labels are listed in Table 3.1.**

The effective device mobilities in the analyses above were calculated using single-sheet mobilities typical of mechanically exfoliated nanosheets ($\mu_0 = 50$ cm^{2}V^{-1}s^{-1}), but other exfoliation processes generate larger and/or distinct defect populations that greatly reduce the sheet mobility. To understand the relative influence of single sheet mobility and edge resistance, Figure 3.7c plots the effective device mobility as a function of both variables. We find that the effective mobility is sensitive to the near-edge resistance even for flake mobilities of a few cm^{2}V^{-1}s^{-1}, *indicating that edge passivation is likely to be beneficial to a wide range of printed thin films*. For example, for a single-sheet mobility $\mu_0 = 2.5$ cm^{2}V^{-1}s^{-1}, reduction of $R_{S,E}/R_S$ from 1000 to 10 results in a 10-fold increase in effective mobility (from 0.1 to 1 cm^{2}V^{-1}s^{-1}). If the single sheet mobility is an optimistic but achievable 25 cm^{2}V^{-1}s^{-1}, a reduction of $R_{S,E}/R_S$ from 1000 to 10 is *necessary* to achieve the target effective mobility.

Reducing the near-edge resistance via passivation not only increases the effective mobility, but also reduces variations in effective mobility with nanosheet density and size (Figure 3.7d), further relaxing constraints on printing. For a given sheet size, the printed density needs to be high enough to avoid large fluctuations that would occur near the threshold for percolation. One can reduce variability between devices by printing at higher densities (towards the right in Figure 3.7d), but the mobility decreases more rapidly in edge-resistance-limited films (Figure 3.7d, upper) than in intersheet resistance limited films (Figure 3.7d, lower). We note that our model is two-dimensional and does not include density fluctuations, so percolation effects are not directly reflected in the plots; the increase in effective mobility at low sheet densities arise from the overlap length becoming comparable to the in-plane screening length, producing large intersheet resistance *and* large near-edge resistance.

Lastly, we consider a scenario where unoptimized exfoliation processes not only generate defective nanosheets with low mobility but also increase the carrier concentration due to electron doping, one example of which is exfoliation via lithium intercalation.[77] The increased carrier concentration not only improves the screening of charged impurities at the nanosheet edges, lowering the expected sheet resistance ratio $R_{S,E}/R_S$ and edge screening length, but also increases the gate screening. Figure 3.9 shows the simulated effective film mobilities when the individual sheet mobility is 5 $cm^2V^{-1}s^{-1}$ (ten times less than in Figure 3.7) and a dopant concentration of 10^{19} cm^{-3} (ten times greater than in Figure 3.7). We find that for the range of $R_{S,E}/R_S$ considered, thinner nanosheets are always desirable (Figure 3.9b).[78] The higher carrier density associated with the higher defect density improves screening of charged impurities such that the reduction in gate screening with decreasing thickness continues to drive a mobility increase. The differences in the effective mobility between edge-resistance- and intersheet-resistance-limited devices also become smaller due to the diminished influence of edge resistance. As was the case in Figure 3.7d, the effective mobility of edge-resistance-limited films is predicted to be more sensitive to variations in printed sheet density and sheet size (Figure 3.9d). While edge passivation will lead to only modest improvements in the average effective mobility, it can greatly reduce variations in the mobility.
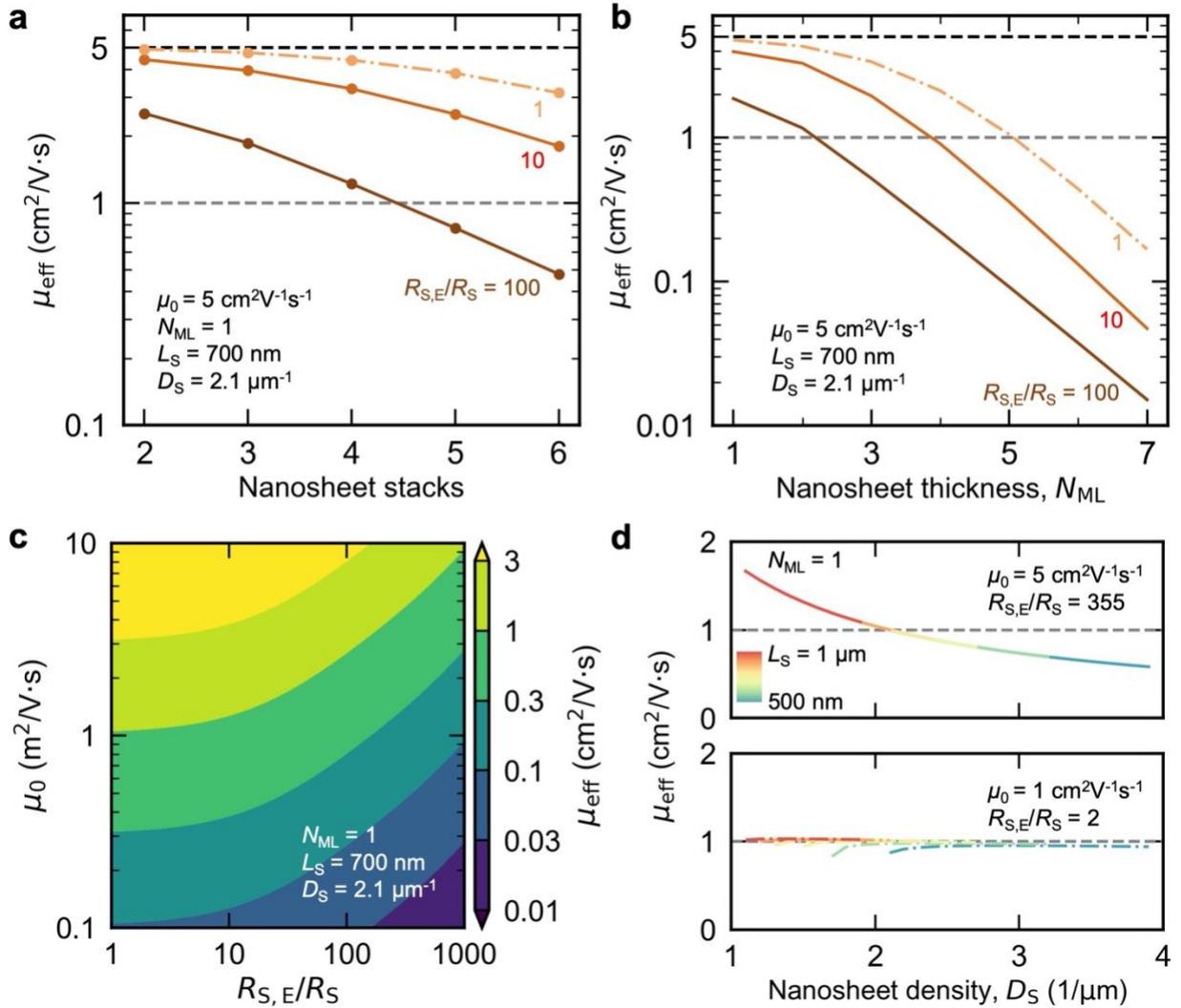
Figure 3.9. Simulation results for printed vdW TFT with lower single-sheet mobilities and higher dopant concentrations. Simulated μ_{eff} vs. (a) number of stacked sheets, (b) nanosheet thickness N_{ML} (*i.e.*, number of monolayers per nanosheet), and (c) single-sheet mobility μ_0 and $R_{\text{S,E}}/R_{\text{S}}$ at the median density $D_{\text{S}} = 2.1 \ \mu\text{m}^{-1}$ (*i.e.*, number of nanosheets per channel length) for nanosheet size $L_{\text{S}} = 700$ nm. (d) Mobility μ_{eff} vs. density D_{S} (color scale: $L_{\text{S}} = 500$ nm-1 μm) for (top) $\mu_0 = 5 \ \text{cm}^2\text{V}^{-1}\text{s}^{-1}$ and $R_{\text{S,E}}/R_{\text{S}} = 355$ and (bottom) $\mu_0 = 1 \ \text{cm}^2\text{V}^{-1}\text{s}^{-1}$ and $R_{\text{S,E}}/R_{\text{S}} = 2$, which are on the $\mu_{\text{eff}} = 1 \ \text{cm}^2\text{V}^{-1}\text{s}^{-1}$ contour line in (c). In (a) and (b), the dot-dashed lines represent $R_{\text{S,E}}/R_{\text{S}} = 1$ (interface-resistance-limited regime), while the solid lines represent $R_{\text{S,E}}/R_{\text{S}} = 10$-$100$ (edge-resistance-limited regime); $\mu_0 = 5 \ \text{cm}^2\text{V}^{-1}\text{s}^{-1}$. In (a), (c), and (d), $N_{\text{ML}} = 1$. In (b)-(d), the number of stacked nanosheets is 3. In all subfigures, the dopant concentration is $10^{19} \ \text{cm}^{-3}$, $\rho_{\text{i,E}}/\rho_{\text{i}} = 1$, and the channel length is 10 μm.

3.6. Perspectives on Processing for Printed vdW TFTs

Our analysis of the influence of nanosheet edges on the effective film mobility provides important perspective on the extant processing methods for printed vdW TFTs. Liquid phase exfoliation employing mechanical sonication in solvents has been used to make inks from many semiconducting 2D materials.[16,31,79,80] Although the individual sheets isolated from these inks exhibit comparable mobilities to those for single-sheet FETs fabricated by tape-assisted exfoliation,[16,79] the printed film mobilities are much lower due to the difficulty in obtaining thin and large sheets. The tip sonication (ref.[16]: 450 W and 1 hour in NMP) necessary to produce thin sheets inevitably reduces the sheet size,[81] typically resulting in 10-20 layer nanosheets that are 300-400 nm.[16,28] These relatively thick and small nanosheets tend to form films with nonplanar stacking and a high concentration of voids (Figure 3.1b purple schematic), requiring multiple layers of printing and thick films to achieve percolation (refs.[15,16,28]: film thickness ~1 μm). Such a microstructure cannot realize the effective mobilities that are possible in thin films with planar stacking. As an alternative, electrochemical exfoliation can preserve larger sheet sizes down to smaller thicknesses,[20–22,26,27] and could be used to produce micron-size 5-6 layer MoS_2 nanosheets[26] that we predict are optimal in the edge-resistance-limited regime (Figure 3.7b). Efforts to produce nanosheets that are thinner than the screening length will only improve performance if the edge states are sufficiently passivated. Indeed, prior studies have shown that thinner nanosheets that undergo similar electrochemical processes as thicker sheets result in lower effective film mobilities (see refs [20,27] and comparisons in Figure 3.7b). Efforts to passivate the basal planes and/or interfaces of MoS_2 films have led to only modest improvements (ref.[28]: 1,4-

benzenedithiol covalent functionalization) or trade-offs between increasing the on/off ratio and decreasing the effective mobility (ref.[20]: TFSI treatment).

The generalization of the electrochemical approach to a broader range of 2D materials beyond MoS_2 is an important direction for printed 2D electronics,[21,26,82] and consideration of how the chemical species used in electrochemical exfoliation affect the edge states could lead to improvements in process design and film performance, particularly for more reactive 2D materials such as p-type black phosphorus[32,79] and n-type InSe.[80] As discussed above, spontaneous oxidation in an ambient environment can lead to negatively charged impurities at nanosheet edges. Hence, for n-type materials, processing strategies should include chemistries that selectively n-dope and/or passivate the edge states to increase the electron concentration locally.[83] For p-type materials in which holes are the majority carriers, film performance might be limited by the positively charged impurities at edges, which can arise from adsorption of cations used in the electrochemical exfoliation,[26] suggesting that processes to remove the ionic species should be developed. For electrochemical exfoliation processes that produce nanosheets with high defect concentrations in the basal plane, the effective film mobility may be low, but it will be less sensitive to defects at edges due to electron doping and can still reach mobilities exceeding 1 $cm^2V^{-1}s^{-1}$ considering that thinner nanosheets reduce gate screening (Figure 3.9). TFTs printed from these more defective nanosheets might still be competitive against amorphous silicon for low-end applications.

3.7. Conclusion

Through the development and calibration of a resistor network model, we analyzed how near-edge and intersheet resistances influence the performance of printed 2D transistors as a function of nanosheet stacking, thickness, size, and density. For mechanically exfoliated MoS_2, the presence of fixed negative charges at nanosheet edges is shown to induce a large local increase in resistance that limits the effective mobility for typical intersheet resistances. When transport in the 2D film that consists of high-mobility and moderately doped nanosheets is limited by the near-edge resistance, rather than the intersheet resistance, there is an optimum nanosheet thickness that can be targeted by exfoliation processes. Successful passivation of edges will enable the realization of higher mobilities with thinner nanosheets due to reduced junction resistances and reduced screening of the gate. For a film assembled from nanosheets that have lower mobility but higher dopant concentration, reducing the nanosheet thickness via development in exfoliation and sorting processes will improve both effective mobility and on/off ratio.

3.8. Extended Analysis

3.8.1. Estimation of μ, R_C and R_J from Transfer Characteristics

The access resistances R were extracted for t-8L, b-8L, and 8L/8L devices by using the Y-function method (Section 2.2). For single-sheet t-8L and b-8L devices ((1-2) and (4-5) in Figure 3.2a, respectively), the R_A was considered to be the contact resistance, giving $R_{A,t-8L} = R_1 + R_2 = 4.3$ kΩ and $R_{A,b-8L} = R_4 + R_5 = 9.7$ kΩ. For the 8L/8L device (electrodes 3-4), the R_A consists of the contact and junction resistances, giving $R_{A,8L/8L} = R_3 + R_4 + R_J = 19.3$ kΩ. Assuming that the two contact resistances on a given nanosheet are equal (*i.e.*, $R_1 = R_2 = R_3$ and $R_4 = R_5$), the junction resistance is given by $R_J = R_{A,8L/8L} - (R_{A,b-8L} + R_{A,t-8L})/2 = 12.3$ kΩ.[64]

The above analysis assumes that the contacts are ohmic and do not limit transport aside from introducing a series resistance. The devices measured here were confirmed to be ohmic by inspecting the linear output curves presented in Figure 3.11, Figure 3.12, and Figure 3.13. The analysis explains why the peak mobility of the 8L/8L homojunction is slightly higher than the bottom-8L. First, the contact resistance of the 8L/8L device is lower than the bottom-8L device. Second, the top-8L in the 8L/8L has a higher mobility than the bottom-8L.

For devices in which the transconductance does not saturate or decrease (Figure 3.12d and Figure 3.13d), the single-sheet mobilities were extracted directly from the field-effect mobilities $\mu_{FE} = (dI_{DS}/dV_{GS})(L/V_{DS}WC_{ox})$ at a particular V_{GS}, assuming that transport is limited by the channel resistance instead of the contact resistance. Table 3.3 summarizes the extracted μ_B, μ_T, and V_{OV} for 8L/8L, 5L/1L, and 1L/1L.
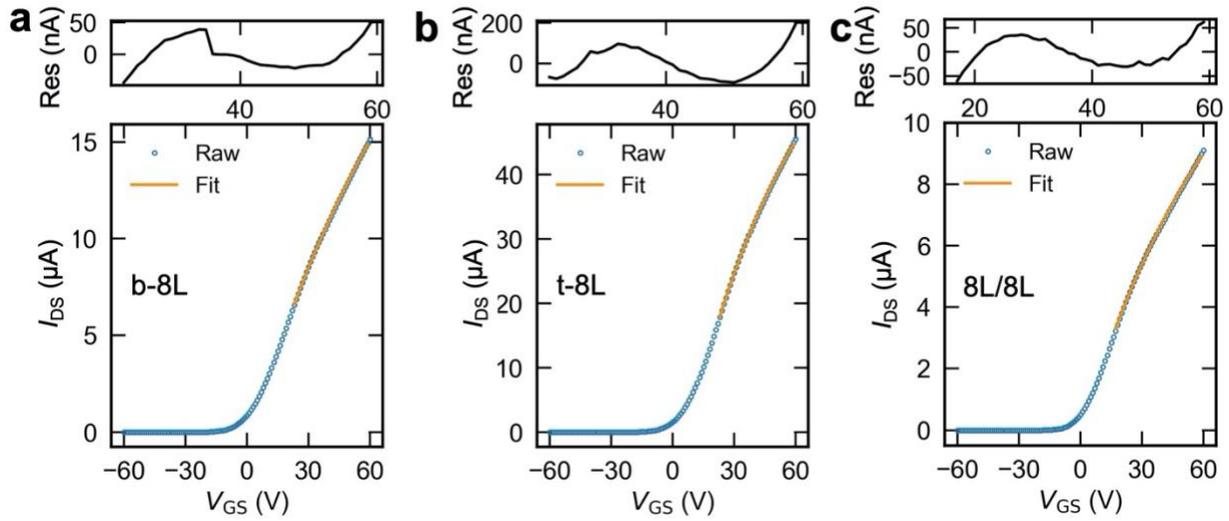
Figure 3.10. Y-function analysis of transfer curves. Residual, raw, and fitted drain-source current I_{DS} vs. gate-source voltage V_{GS} for (a) bottom-8L, (b) top-8L, and (c) 8L/8L devices.

Table 3.3. Summary of extracted μ_B, μ_T, and V_{OV} for 8L/8L, 5L/1L, and 1L/1L.

Homojunction device	μ_B (cm^{2}V^{-1}s^{-1})	μ_T (cm^{2}V^{-1}s^{-1})	V_{OV} (V) at applied V_{GS}
8L/8L	44.6	84.2	2.4 at $V_{GS} = 0$ V
5L/1L	33.7	42.9	9.4 at $V_{GS} = 20$ V
1L/1L	21.5	21.1	0.5 at $V_{GS} = 30$ V

Note: the mobilities for 8L/8L were extracted using the Y-function method (Section 2.2), while those for 5L/1L and 1L/1L were extracted from the transconductance/μ_{FE} at $V_{GS} = 20$ V and 30 V (Figure 3.12d and Figure 3.13d), respectively, where the surface potential profiles were measured. The overdrive voltage V_{OV} was determined at the applied V_{GS} where surface potentials were measured (Equation 2.2).

3.8.2. KPFM Resolution and Bias Conditions

The spatial resolution of KPFM was estimated to be ~300 nm from the lateral spread in the CPD profile near the exposed edge of the top-5L on top of the bottom-1L (Figure 2.7). We note that the potential drop produced by the wrinkle in Figure 3.3b is comparable to the potential resolution, suggesting that its impact on the potential drop near the buried edge of the 8L/8L junction is negligible.

KPFM data in both moderate accumulation and depletion were acquired for all devices based on the transfer curves. The transfer curve in Figure 3.2c shows that the 8L/8L device begins to turn on at V_{GS} = -30 V, shows moderate accumulation at V_{GS} = 0 V, and is fully depleted at V_{GS} = -45 V. As noted in the manuscript, we did not bias the 8L/8L to higher V_{GS} to keep the current density low and minimize oxidation during KPFM measurement in air (KFPM measurements take much longer than a single bias sweep). For the 5L/1L device, the transfer curve in Figure 3.12c shows that the device begins to turn on at V_{GS} = -10 V, shows moderate accumulation at V_{GS} = 20 V, and is depleted at V_{GS} = -20 V. For the 1L/1L, the transfer curve in Figure 3.13c shows that the device started to turn on at V_{GS} = ~0 V, showing accumulation at V_{GS} = 30 V and depletion at V_{GS} = -30 V.

3.8.3. Extended electrical, KPFM, and Raman data
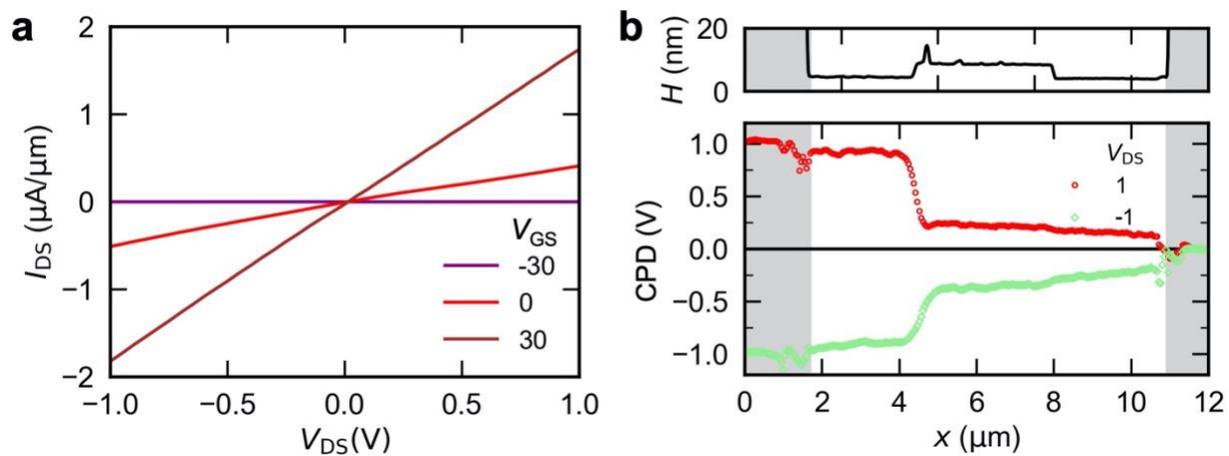
Figure 3.11. Extended device characteristics of 8L/8L. (a) Output curves I_{DS} vs. V_{DS} at different V_{GS}. (b) CPD profiles at $V_{DS} = \pm 1$ V and $V_{GS} = 0$ V.
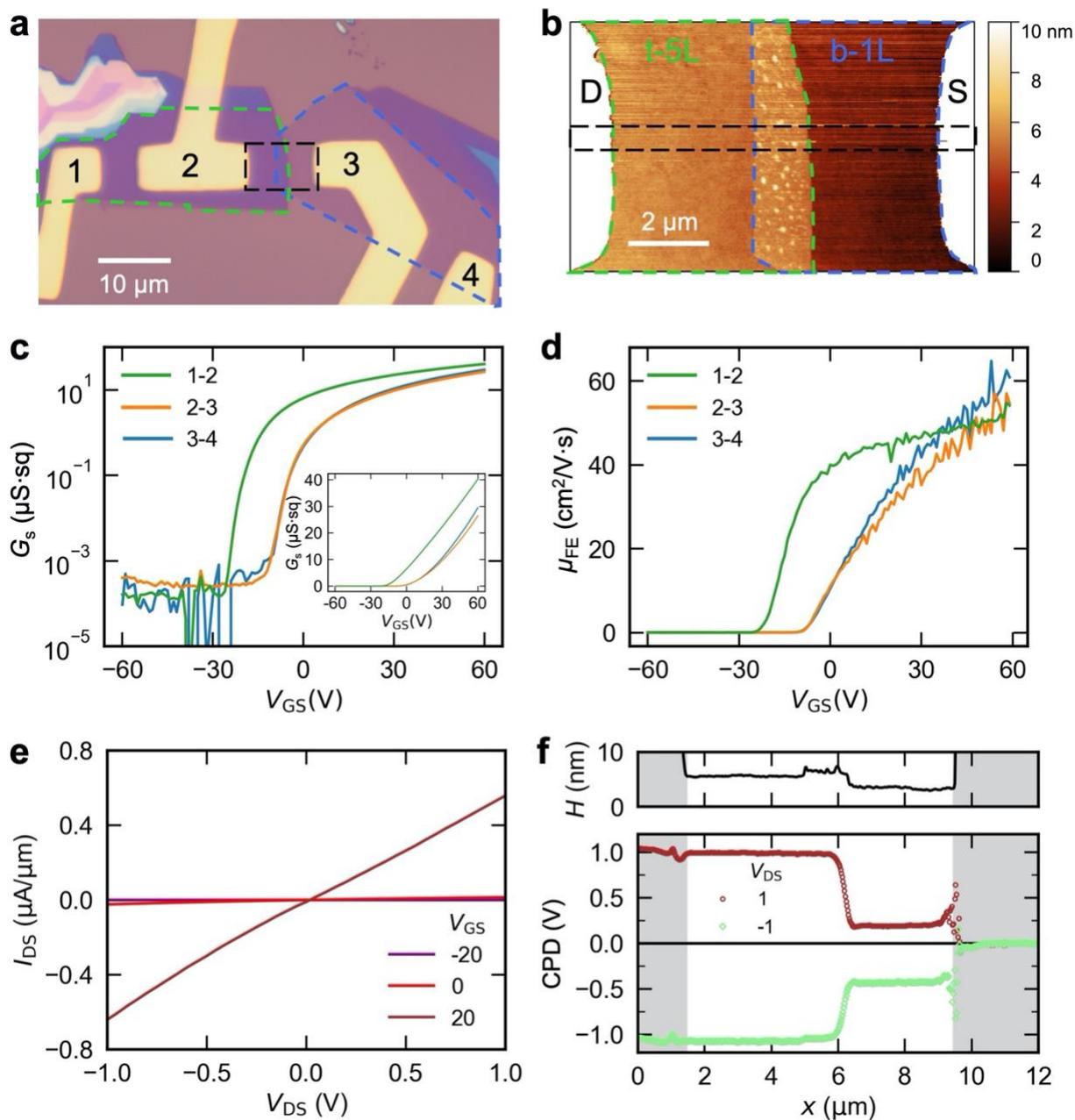
Figure 3.12. Characterization of 5L/1L device. (a) Optical microscope image of the single-nanosheet and homojunction devices. **(b)** AFM topography of the region indicated by a black dashed square in (a). **(c)** Sheet conductance G_S vs. V_{GS} and **(d)** field-effect mobility μ_{FE} vs. V_{GS} for the devices shown in (a) at $V_{DS} = 0.5$ V. **(e)** I_{DS} vs. V_{DS} for 5L/1L at different V_{GS}. **(f)** CPD profiles at $V_{DS} = \pm1$ V and $V_{GS} = 20$ V.
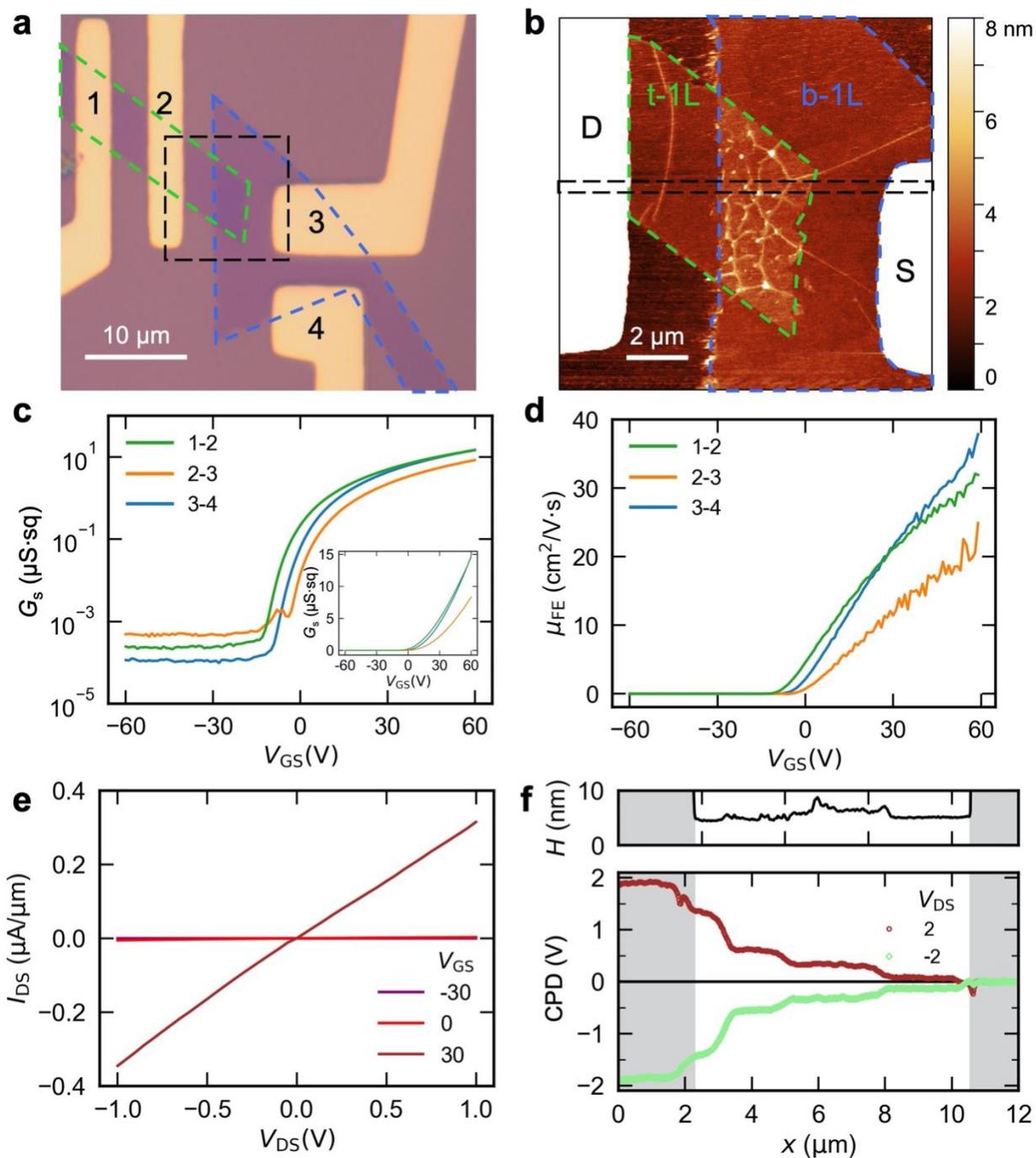
Figure 3.13. Characterization of 1L/1L device. (a) Optical microscope image of the single-nanosheet and homojunction devices. (b) AFM of the region indicated by a black dashed square in (a). (c) G_S vs. V_{GS} and (e) μ_{FE} vs. V_{GS} for the devices shown in (a) at $V_{DS} = 0.5$ V. (e) I_{DS} vs. V_{DS} for 1L/1L at different V_{GS}. (f) CPD profiles at $V_{DS} = \pm 2$ V and $V_{GS} = 30$ V.
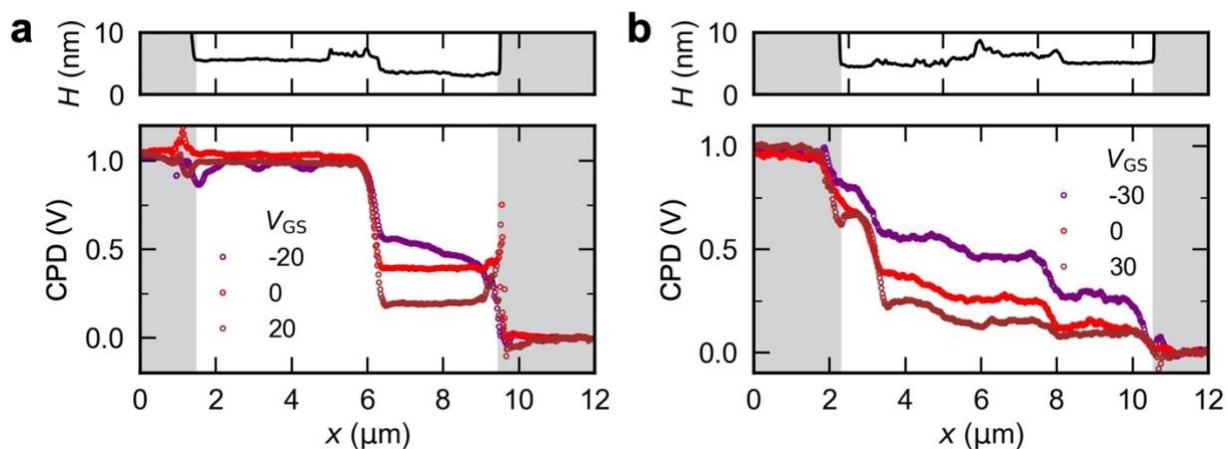
Figure 3.14. Gate-dependent CPD profiles for (a) 5L/1L device and (b) 1L/1L at $V_{DS} = 1$ V.
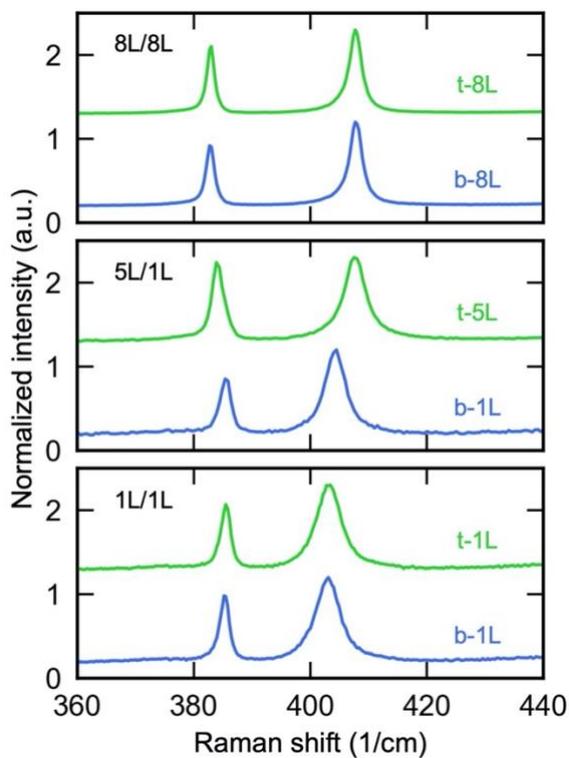
Figure 3.15. Raman spectra of the nanosheets used in 8L/8L (top), 5L/1L (middle), and 1L/1L (bottom). All nanosheets are 2H-phase MoS₂.

3.8.4. Extended sensitivity analysis

Different near-edge resistance ratios for the top and bottom nanosheets were used to simulate the junction resistance R_J for the 8L/8L device. The near-edge sheet resistance ratio for the b-8L $R_{B,BE}/R_B$ and intersheet resistance ratio $\rho_{i,E}/\rho_i$ are coupled; increasing $R_{B,BE}/R_B$ results in a smaller $\rho_{i,E}/\rho_i$ for the same R_J. In all cases, the near-edge sheet resistance ratio for the t-8L $R_{T,BE}/R_T = R_{T,EE}/R_T$ is greater than 2000, indicating that the dominant contributor to the junction resistance is the near-edge sheet resistance of the t-8L device (Figure 3.16), as described in the main text.
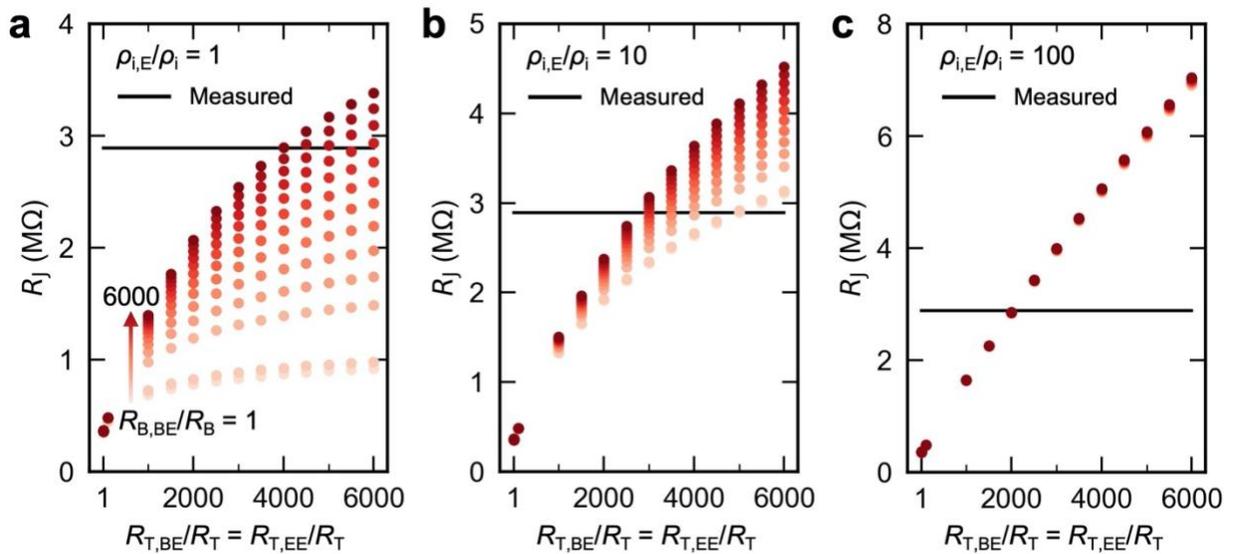
Figure 3.16. Extended parameter sensitivity analysis of the model for the 8L/8L device. Simulated junction resistance R_J vs. t-8L near-edge sheet resistance ratio $R_{T,BE}/R_T = R_{T,EE}/R_T$ at $R_{B,BE}/R_B = 1\text{-}6000$ and at $\rho_{i,E}/\rho_i = $ (a) 1, (b) 10, and (c) 100. The black lines represent the experimentally estimated junction resistance. Note that $R_{B,EE}/R_B = 1$ for the 8L/8L device.

Chapter 4   Origin of the Photoresponse in Printed MoS$_2$ Photodetectors

4.1.   Introduction

2D material inks have potential applications beyond TFT such as photodetection,[17,21,74,76] chemical sensing,[22,84] and energy storage.[85] In Spring 2021, Lidia Kuo from the Hersam Group at NU demonstrated all-printed MoS$_2$ photodetectors with ultrahigh-responsivity, while Ting-Ching Chu from the Lauhon Group performed scanning photocurrent microscopy (SPCM) and spectroscopy on their devices to determine the origins of the photoresponse. To interpret the SPCM measurements, the author used optical microscopy-based methods to determine the device topography and confirmed the photoconductive behavior using local photoimpedance spectroscopy. This set of characterization methods established the origin of the photoresponse and its sensitivity to variations in processing conditions, informing the development of processing conditions that optimize photodetection performance.

Part of the work documented in this chapter has been published in Advanced Materials in 2022 by Lidia Kuo, Vinod K. Sangwan, Sonal V. Rangnekar, Ting-Ching Chu, David Lam, Zhehao Zhu, Lee J. Richter, Ruipeng Li, Beata M. Szydłowska, Julia R. Downing, Benjamin J. Luijten, Lincoln J. Lauhon, and Mark C. Hersam.[76]

4.1.1.   Ultrahigh-Responsivity of Aerosol-Jet Printed MoS$_2$ Photodetectors

As detailed in ref. [76], few-layer MoS$_2$ nanosheets were electrochemically exfoliated from bulk crystals[26], formulated into a printable ink with a stabilizing polymer, and printed using an aerosol-jet printer onto polyimide substrates with pre-printed graphene contacts; the MoS$_2$ channel was typically printed on top of the graphene contacts. The printed device was either photonically

annealed with a Xenon lamp (4.06 J cm^{-2} for 1.36 ms) or thermally annealed in a tube furnace (280 °C with 50 sccm Ar flow).[76] Optical micrographs of the printed and annealed devices are shown in Figure 4.1a,b. The photonically annealed devices showed responsivities exceeding 10^3 AW^{-1}, which outperformed previously reported all-printed visible-light photodetectors by over three orders of magnitude.[17,76] The superior photoresponsivity was primarily attributed to the intimate intermixing of graphene and MoS$_2$ nanosheets at the channel-contact interface, resulting in quasi-ohmic contacts and possibly greater nanosheet interconnectivity across the channel.[76]

4.1.2. Scanning Photocurrent Microscopy – Where Does the Photocurrent Arise?

Full-device illumination is useful for establishing the performance in real world conditions, but it does not provide insight into the operating principles, which is crucial for rational optimization. To determine the origin of the photocurrent, Ting-Ching Chu performed SPCM (wavelength λ = 630 nm, spot size = 1.54 µm) on both the photonically annealed and thermally annealed devices. The SPCM results revealed that the photocurrent was larger near the top and bottom of the channel than in the middle for both devices (Figure 4.1c,d). One possible explanation for this result is that the thicker regions of the film absorb more light, but this hypothesis needs to be tested by characterizing the thickness variations. Additionally, the photocurrent was found to be larger in the MoS$_2$ channel than at the graphene electrodes (Figure 4.1e,f). To interpret the photocurrent mechanism, it is important to distinguish the photoresponse between the channel and the contacts, which requires determining the exact locations of the contacts.
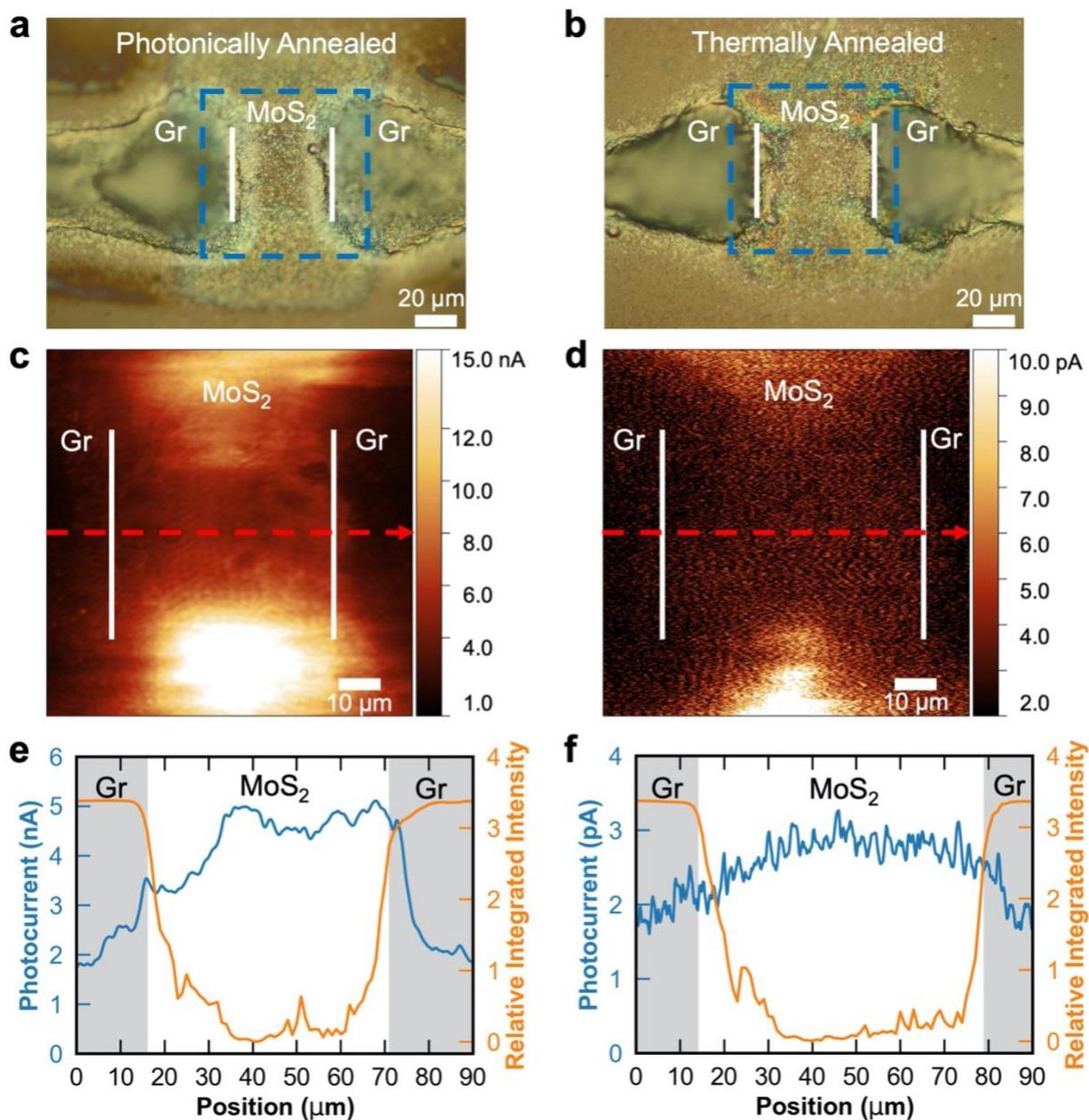
Figure 4.1. Scanning photocurrent microscopy (SPCM) characterization of printed MoS$_2$ photodetectors. Optical micrographs of representative (a) photonically annealed and (b) thermally annealed devices. The corresponding SPCM maps of the blue dashed squares for (c) the photonically annealed device measured at a 4 V bias, and (d) the thermally annealed device measured at a 5 V bias with a 630 nm laser (spot size = 1.54 μm, power = 41 μW). The corresponding horizontal profiles of photocurrent and relative integrated Raman intensities for the (e) photonically annealed and (f) thermally annealed devices, extracted at the red dashed lines in (c) and (d). The grey areas denote the graphene contact regions.

4.2. Optical Determination of Device Topography to Interpret SPCM

Interpretation of the SPCM requires spatially correlating the photocurrent magnitude with the device topography. Considering that it was challenging to measure the device topography with the conventional tapping-mode AFM technique, non-contact optical methods were explored to construct the relative height profiles of the printed devices.

4.2.1. Challenges in Measuring Topography of Printed Film with AFM

There are two main challenges associated with measuring the topography of printed devices using conventional tapping-mode AFM. Firstly, the printed film is composed of percolating nanosheets with weak intersheet vdW interactions that may slide due to interaction with the AFM tip.[86] Secondly, the printed channel lengths are typically more than 50 µm, which makes scanning the topography with AFM an inefficient process. Therefore, non-contact high-throughput characterization methods need to be developed for these large, printed devices.

4.2.2. Constructing Relative Height Profiles via Optical Methods

Two far-field optical scattering-based methods were utilized to construct the relative height profiles of the printed MoS_2 devices, including white light interferometry (3D optical microscopy) and measuring inelastic scattering from the polyimide substrate.

4.2.2.1. White Light Interferometry to Measure Thickness Variations in Channel

A white light interferometer (WLI), which is also referred to as a 3D optical microscope or optical profilometer (Figure 4.2a), utilizes a Mirau interferometric objective to reveal the sample

surface via an interference pattern only when the proper focus is reached. In the interferometric objective, a broadband "white light" source is split into reference and measurement beams by a beam splitter. The reference beam is reflected by a reference mirror, while the measurement beam is reflected or scattered from the sample surface (Figure 4.2b). The returning beams are relayed to a detector by the beam splitter and form an interference pattern, or fringes, of the sample's surface topography that is spatially sampled by individual CCD pixels (Figure 4.2a). The interference pattern (*i.e.*, fringes) only appears in the CCD where the optical path lengths of beams differ by less than half the coherence length of the light source, which is typically on the order of a micrometer. The objective is moved vertically to find the position of maximum fringe contrast for each pixel, which corresponds to the focus position of a particular point on the sample surface. The encoder records the relative objective-to-sample distance as the "height" information, while the camera records the spatial location.

It should be noted that the relative "height" measured by WLI is not the geometrical height of the sample. Instead, it is a measure of the optical path difference; optical path length OPL = ns, where n is the refractive index and s is the geometrical length/thickness. For materials with the same refractive index, such as multilayer MoS_2, the optical path difference can be used to construct the geometrical topography. However, for materials with different refractive indexes, such as MoS_2 and SiO_2, the "height" measured by WLI cannot be used to interpret the topography. Similar to conventional optical microscopy based on reflective illumination, the contrast of WLI also depends on the optical path difference, which can be sub-nanometer.[87] For example, WLI can resolve monolayer graphene on SiO_2/Si. The lateral resolution Δl, which is typically sub-micron,

is determined by the Rayleigh criterion: $\Delta l \approx 1.22 f\lambda/D$, where λ is the wavelength of the light source, f is the focal length of the objective, and D is the diameter of the aperture.

In the case of printed MoS_2 devices on polyimide, WLI (Bruker ContourGT) was utilized to measure the thickness variations in the MoS_2 channel by assuming that the printed film has a bulk-like refractive index. The 3D optical micrographs of the photonically annealed (Figure 4.2c) and thermally annealed (Figure 4.2d) devices showed that the channel is thicker near the top and bottom than in the middle. For both devices, the top and bottom areas are approximately 100-200 nm thicker than the middle of the channel (Figure 4.2e,f), which results in increased light absorption and photoexcited carrier generation. However, it is expected that carrier collection will be more efficient in the middle of the channel than near the top and bottom because the electric field is largest and parallel to the channel. Therefore, future process development can focus on producing a uniform channel thickness to improve both absorption and carrier collection, resulting in better photocurrent homogeneity and overall photocurrent density in the channel.

Furthermore, the photonically annealed MoS_2 film (RMS roughness = 58 nm in the middle of the channel) is rougher than the thermally annealed film (RMS roughness = 33 nm). Photonic annealing differs from thermal annealing in its use of a high-intensity, broadband spectrum of pulsed light to locally and rapidly heat the light-absorbing MoS_2 and graphene on the thermally insulating polyimide substrate.[17] Thus, photonic annealing leads to a rougher film morphology as a result of the rapid gas evolution during the decomposition of polymeric species present in the as-printed film.
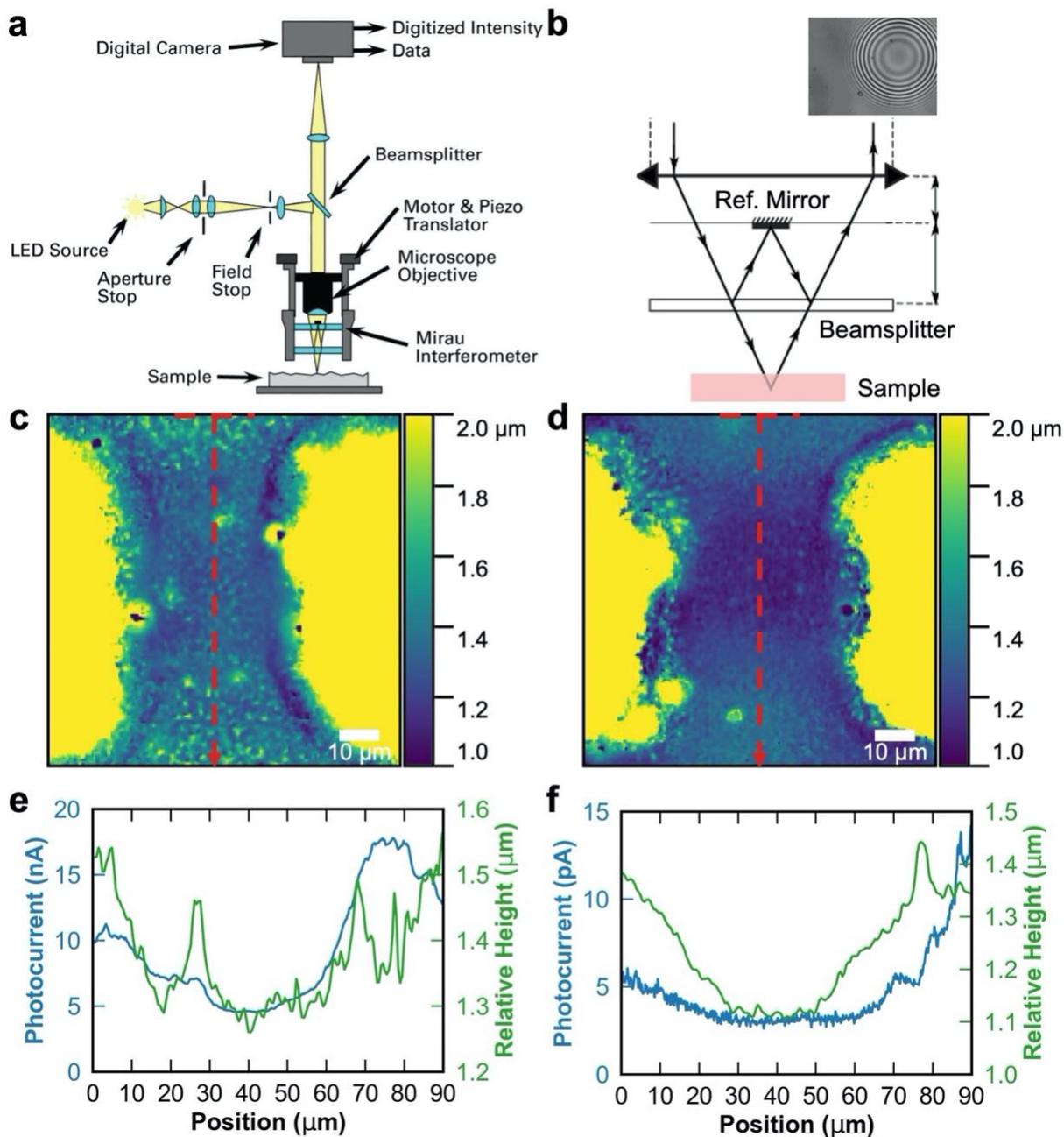
Figure 4.2. White light interferometry to measure thickness variations in the channel. (a) Schematic of a white light interferometer. Credit to Bruker Nano Surfaces. (b) Schematic of a Mirau interferometric objective. 3D optical micrographs of the area scanned in SPCM measurements for the (c) photonically annealed and (d) thermally annealed devices. The corresponding photocurrent and relative height profiles of the (e) photonically annealed and (f) thermally annealed devices, averaged across 20 μm width along the red lines in (c) and (d).

4.2.2.2. Raman Profiling of Polyimide Substrate to Determine Contact Locations

To correlate the SPCM data to the graphene contacts and MoS$_2$ channel, Raman profiling (Horiba LabRAM HR Evolution) was performed along the device (Figure 4.3a). The polyimide substrate generates broad background scattering that is attenuated by the graphene contacts (Figure 4.3b-e). By selecting a frequency range where the attenuation occurs primarily via absorption with negligible reflection and diffuse scattering, the transmitted substrate scattering signal can be used to calculate the relative graphene thickness based on the Beer-Lambert law: $\alpha t = \log(I_0/I_T)$ and $I_0/I_T \approx I_{max}/I_X$, so $t \propto \log(I_{max}/I_X)$, where α is the absorption coefficient, t is graphene thickness, I_0 is the incident intensity to the graphene, I_T is the transmitted intensity through the graphene, I_{max} is the maximum Raman intensity from the polyimide along the scan, and I_X is the Raman intensity from the polyimide along the scan. The intensities from the polyimide, I_{max} and $\underline{I}_X$, were calculated by integrating the counts between 2000 cm^{-1} and 3000 cm^{-1}, which are attributed only to the inelastic scattering by polyimide (Figure 4.3b). By plotting the relative integrated intensity against the photocurrent profile (Figure 4.1e,f), we can determine the contact locations and confirm that the photoresponse primarily arises from the MoS$_2$ channel. Hence, it can be inferred that the device behaves as a photoconductor, where the conductivity of the channel increases due to excess free carriers.
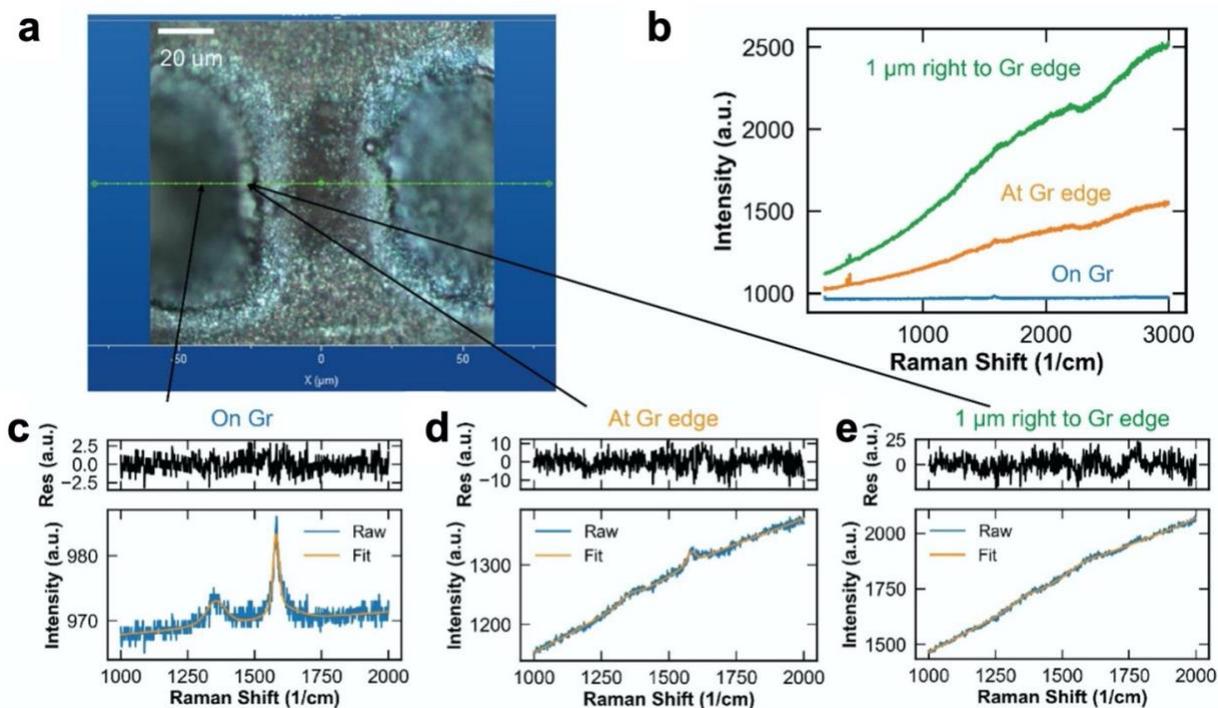
Figure 4.3. Raman profiling of polyimide substrate to determine the contact locations. (a) Optical image of a printed MoS₂ photodetector, showing zoomed-in channel and contact regions. (b) Raman spectra acquired at various locations on the device. (c) Raman spectrum at the graphene contact, showing characteristic D and G bands. (d) Raman spectrum at the graphene edge, where the D and G bands are less intense. (e) Raman spectrum away from the graphene edge, showing large background intensity from the polyimide substrate. The raw spectra can be found in the MDF: kuo_mos2_mse**.**

4.3. Confirmation of Photoconductive Behavior by Photoimpedance Spectroscopy

The combination of SPCM and non-contact optical characterization of device topography helped establish the DC photocurrent generation mechanisms for printed MoS₂ photodetectors. At the time, collaborative work between the Hersam group at NU and the Air Force Research Laboratory demonstrated ultrasensitive gas detection in printed MoS₂ devices with Au contacts using impedance-based measurements.[84] This work raised the question of whether operating the

printed MoS$_2$ photodetectors with graphene contacts (Figure 4.1a,b) at an AC frequency produces a capacitive photoresponse that improves the photodetection sensitivity. Additionally, tunable capacitors have important applications in setting the resonance frequency in L/C circuits and tuning the reactance for impedance matching. Four main technologies for tunable capacitors include dielectric variable capacitors, varactor diodes, micromachined capacitors, and integrated transistor-switched capacitors based on complementary metal–oxide–semiconductor (CMOS).[88] Among these technologies, optically tunable capacitors offer one of the simplest system designs and enable future circuit miniaturization.

To explore the possible use case of printed MoS$_2$ devices as AC photodetectors, photoimpedance spectroscopy with local photoexcitation was performed. A pair of low-impedance co-axial probes (Quarter Research & Development, A-20338, RF/microwave impedance = 50 Ω, frequency range = 0-18 GHz) were placed ~500 μm apart and used to contact the graphene electrodes (Figure 4.4a). Shielded BNC cables were used to connect the probes to the impedance analyzer (Solartron Analytical 1260). The contacts and the channel were selectively illuminated with a divergent 532 nm laser beam (spot size ≈ 18 μm, power ≈ 10 μW) while measuring the frequency-dependent impedance and phase shift. An equivalent circuit for the measurement consists of a parasitic capacitance in parallel with a parasitic resistance and the sample (Figure 4.4b).[55] Detailed descriptions of how impedance spectra were measured can be found in Chapter 2 Section 2.4.

Figure 4.4c,d shows the impedance spectra with and without illuminating the channel and the parasitic impedance measured by lifting probes from the graphene contacts. For a pure resistor, the impedance $Z = R$ with no phase shift, where R is the resistance. For a pure capacitor, $Z = 1/(j\omega C)$

with a -90° phase shift (*i.e.*, the voltage lags the current by 90°), where C is the capacitance. Thus, the parasitic capacitance, $C_{para} = 0.3$ pF, was extracted by performing a linear fit to the imaginary component at frequencies above 10 kHz, as the parasitic impedance exceeds the instrument limitations below 10 kHz. Only when the device capacitance is comparable to or greater than the parasitic capacitance will the measured imaginary impedance become lower than the parasitic impedance at high frequencies. However, when comparing the impedances above 10 kHz, we observed that the measured imaginary impedance of the probes is comparable to the parasitic impedance (Figure 4.4c), which indicates that the device capacitance is much smaller than the parasitic capacitance since the device and the parasitic capacitance are in parallel.

At lower frequencies, the impedance of the parasitic capacitance increases, and the device resistance dominates the impedance of the parallel circuit, resulting in a real impedance larger than the imaginary impedance (Figure 4.4d). The pure resistive behavior of the device was further confirmed by the 0° phase angle below 1 kHz (Figure 4.4e). The impedance-based photosensitivities $|Z_{Dark}|/|Z_{Light}|$ between 10-1000 Hz are estimated to be 10.3, 4.2, and 3.1 for the channel, right contact, and left contact, respectively (Figure 4.4f). These values are comparable to the peak DC photosensitivities R_{Dark}/R_{Light} at the same locations (Figure 4.4g). Therefore, we conclude that the printed MoS_2 device with graphene contacts essentially behaves as a photoconductor, confirming our inference from SPCM. The MoS_2 and graphene likely form an ohmic junction, which has a negligible capacitance that is usually associated with a depletion region. The formation of ohmic contacts likely contributes to the enhanced photoresponsivity observed in the photonically annealed device. Printing the MoS_2 channel on Au contacts, which form a Schottky barrier,[89] may be a viable approach to enable photocapacitive response.
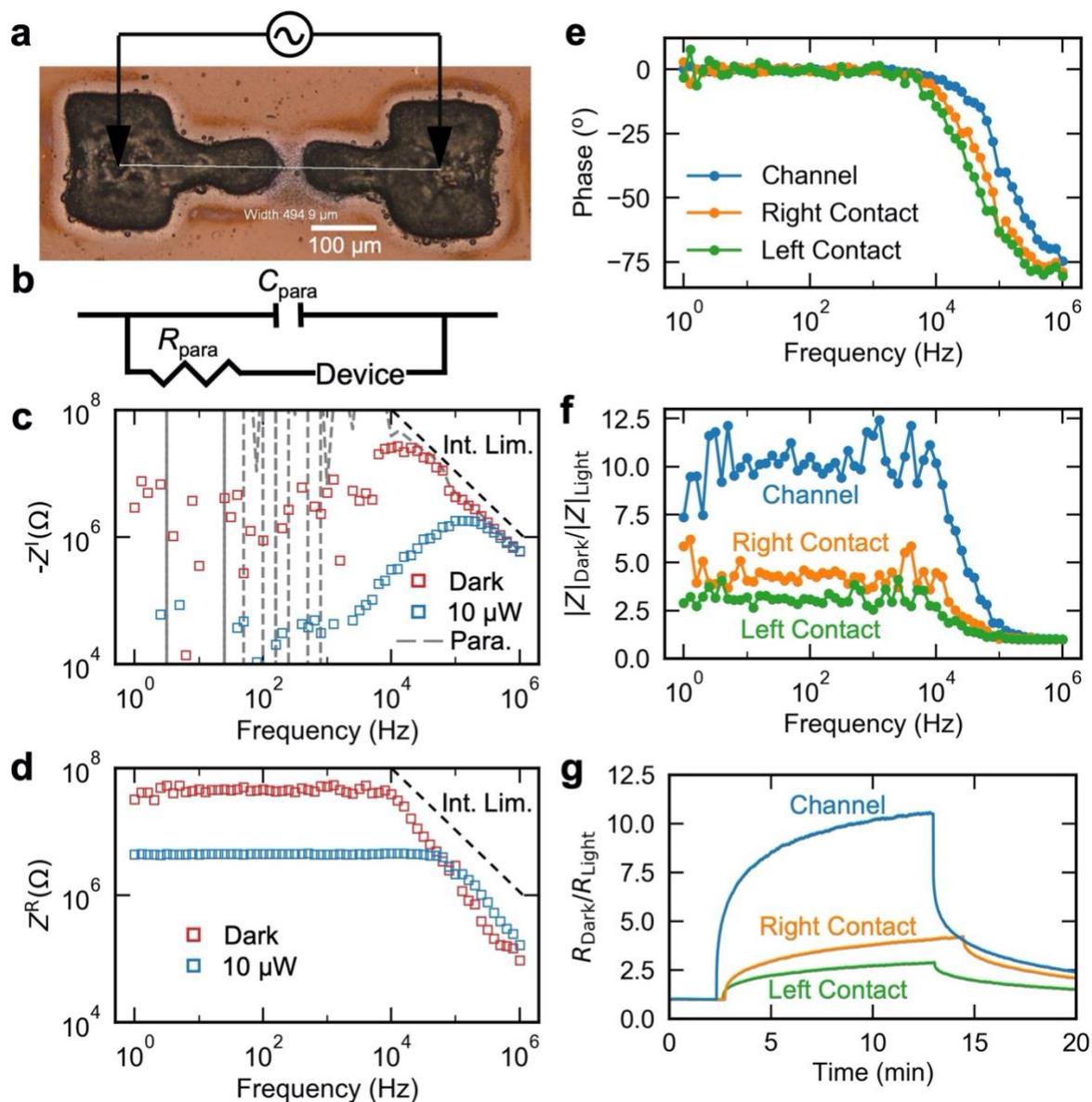
Figure 4.4. Confirmation of photoconductive behavior by photoimpedance spectroscopy. (a) Optical micrograph of the printed MoS$_2$ device with graphene contacts. (b) Equivalent circuit for the impedance measurement. (c) Imaginary $-Z^I$ and (d) real Z^R components of the impedance vs. frequency for the channel in dark and with illumination. The grey dashed line represents the parasitic impedance taken by lifting the probes. The black dashed line represents the instrument limitation. (e) Phase, (f) impedance-based photosensitivity $|Z_{Dark}|/|Z_{Light}|$, and (g) DC photosensitivity R_{Dark}/R_{Light} for the channel, right contact, and left contact, respectively. Local illumination was performed with a divergent 532 nm laser beam (spot size $\approx$ 18 μm, power $\approx$ 10 μW).

4.4. Conclusion

In summary, we characterized the topography of printed MoS_2 photodetectors using optical microscopy-based methods and verified the photoconductive behavior through local photoimpedance spectroscopy. Raman profiling of the polyimide substrate identified the contact locations, confirming that the photoresponse primarily originates from the MoS_2 channel. White light interferometry revealed that the inhomogeneous photoresponse in the MoS_2 channel is due to thickness variations, which are likely caused by the photonic annealing method. Local photoimpedance measurements at the contacts showed negligible capacitance between the graphene contacts and the MoS_2 channel, confirming the formation of an ohmic junction, which likely contributes to the enhanced photoresponsivity of the photonically annealed devices.

Chapter 5   Development of Processing for Printed vdW TFTs

5.1.   Introduction

In our previous publication (Chapter 3),[1] we discovered that the nanosheet edges, not the intersheet resistance, limit transport in printed vdW TFTs. Our model suggests that in a 2D material network consisting of high-mobility and moderately doped nanosheets that produce near-edge resistance, the optimum nanosheet thickness is dictated by a trade-off between charged impurity screening and gate screening, and the film mobilities are sensitive to variations in printed nanosheet density.[1] Our predictions suggest that the removal or passivation of edge states will realize higher film mobilities with thinner nanosheets due to reduced junction resistances and gate screening.[1] In Section 5.2, I discuss the preliminary results and future directions in developing edge functionalization schemes for printed MoS_2 TFTs. We also predicted that to achieve the target mobility of 10 $cm^2V^{-1}s^{-1}$, the printed film thickness must be less than five stacked nanosheets, and even thinner films should be pursued if near-edge resistance is substantial.[1] However, in practice, thinner films may contain voids, which can result in insufficient percolation and reduced conductivity. To address this issue, Section 5.3 outlines the principles and approaches of developing interlayers that can physically and electronically bridge the nanosheets to enhance the percolation of printed thin films.

5.2.   Development of Edge Functionalization for Printed MoS_2 TFTs

Based on the discovery that near-edge resistances limit transport at the junction, we collaborated with Brendan Kerwin from the Marks group to develop functionalization techniques that selectively passivate and/or n-dope the edge states to increase the electron concentration

locally. Our investigation focused on how functional groups impact the local structure and electronic properties of a model 4L/5L MoS_2 homojunction with an exposed step edge (Figure 5.1a,b), where the nanosheet was mechanically exfoliated onto an Au substrate. It has been observed in TEM that MoS_2 nanosheet edges contain a higher density of sulfur vacancies than the basal plane.[28,36] Thus, we initially attempted to use α-lipoic acid (LA), which contains the 1,2-dithiolane functional group predicted to covalently bind to sulfur vacancies.[36,90]

The functionalization involved immersing the MoS_2 sample in α-lipoic acid/IPA for 48 hr, followed by rinsing with IPA and drying with N_2. Contrary to our expectations that the molecules would selectively bind to the edges, we observed their presence on both the basal plane and edges of MoS_2 after functionalization (Figure 5.1c). Additionally, the phase map (Figure 5.1d) and histogram (Figure 5.1e) show distinctive phases for MoS_2 and the molecules. By fitting the peaks to two Gaussian functions (Figure 5.1e), we estimated that the coverage of the molecules on the surface is $34 \pm 1\%$ by:

$$Coverage = \frac{A_{\text{LA}}}{A_{\text{MoS}_2} + A_{\text{LA}}}$$

(5.1)

where A_{LA} and A_{MoS_2} are the integrated peak areas for the molecules and MoS_2, respectively. Assuming that the physically adsorbed species are removed by the IPA rinse, leaving only covalently bonded species remain on the surface, the basal plane likely contains a sufficiently high density of sulfur vacancies that bind to the molecules; previous work has shown that the density of sulfur vacancies on the basal plane of mechanically exfoliated MoS_2 is $(1.2 \pm 0.4) \times 10^{13}$ cm^{-2}.[91]
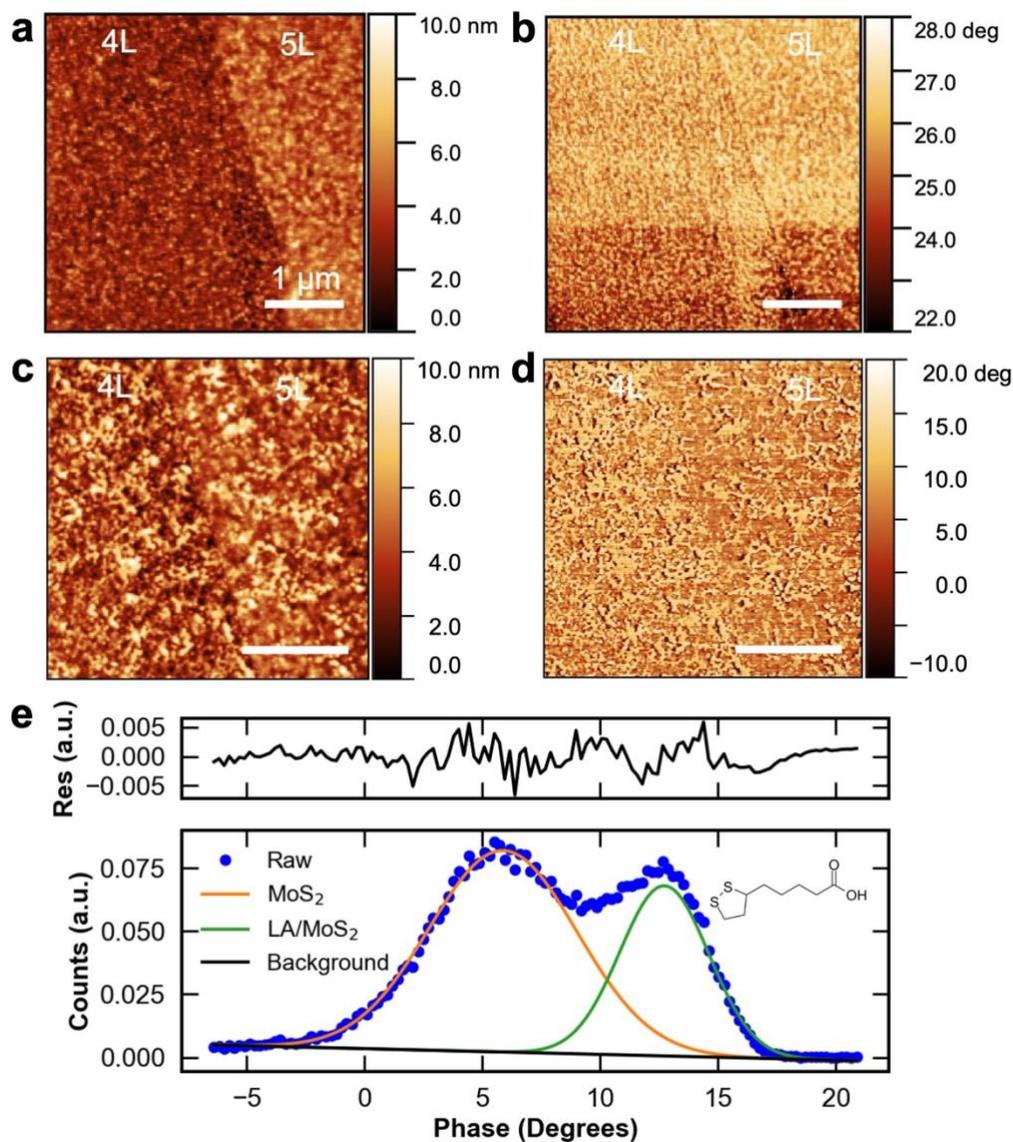
Figure 5.1. Topographic change after α-lipoic acid (LA) functionalization. AFM (a) surface topography and (b) phase maps of the 4L/5L MoS₂ before functionalization. (c) Surface topography and (d) phase maps after functionalization LA. The scale bar is 1 μm. (e) Phase histogram after functionalization. The curve was fitted by two Gaussian functions with a linear background. The inset shows the molecular structure of LA.

We used KPFM to investigate the impact of functionalization on the work function. The surface potentials of as-exfoliated 5L and 4L are comparable (Figure 5.2a,b), indicating flat-band conditions for both (Figure 5.2c). The surface band bending of the few-layer MoS_2 is modified after functionalization, resulting in a 60 meV higher potential for 5L compared to 4L (Figure 5.2d,e). This observation suggests that the functionalized molecules bind to sulfur vacancies on the surface of MoS_2, lowering the Fermi level and increasing the work function (Figure 5.2f).[92]

Edge-selective functionalization requires designing a molecule with functional groups that exhibit distinct interactions with edge sites and the basal plane. For instance, a chemically reactive functional group (*e.g.*, 1,2-dithiolane for MoS_2 functionalization) could be attached to a long, non-polar chain (*e.g.*, alkyl).[83] In order for the molecule to chemisorb at defect sites, it must rotate to align the reactive group with the defect; however, the alkyl chain could introduce steric hindrance to this rotation. At the edges, where defect density is higher, the reactive group may bind to defect sites with lower activation energy and faster kinetics. Conversely, on the basal plane, physisorption of the alkyl chain with the vdW surface may be promoted. Physically adsorbed species can either diffuse on the basal plane to the reactive edge sites[93] or be removed by rinsing, leaving only the edge sites functionalized. Furthermore, it is essential to recognize that edge chemistry may be environment-dependent, and the choice of functionalization agent should be carefully considered. Our initial strategy was based on TEM observations, typically conducted in high vacuum with mild sample annealing, that sulfur vacancies are abundant at MoS_2 edges.[28,36] However, oxidation of the edges is expected under ambient conditions, [67–70] necessitating the development of a mild reducing agent to passivate edge states and locally increase electron concentration.[83]
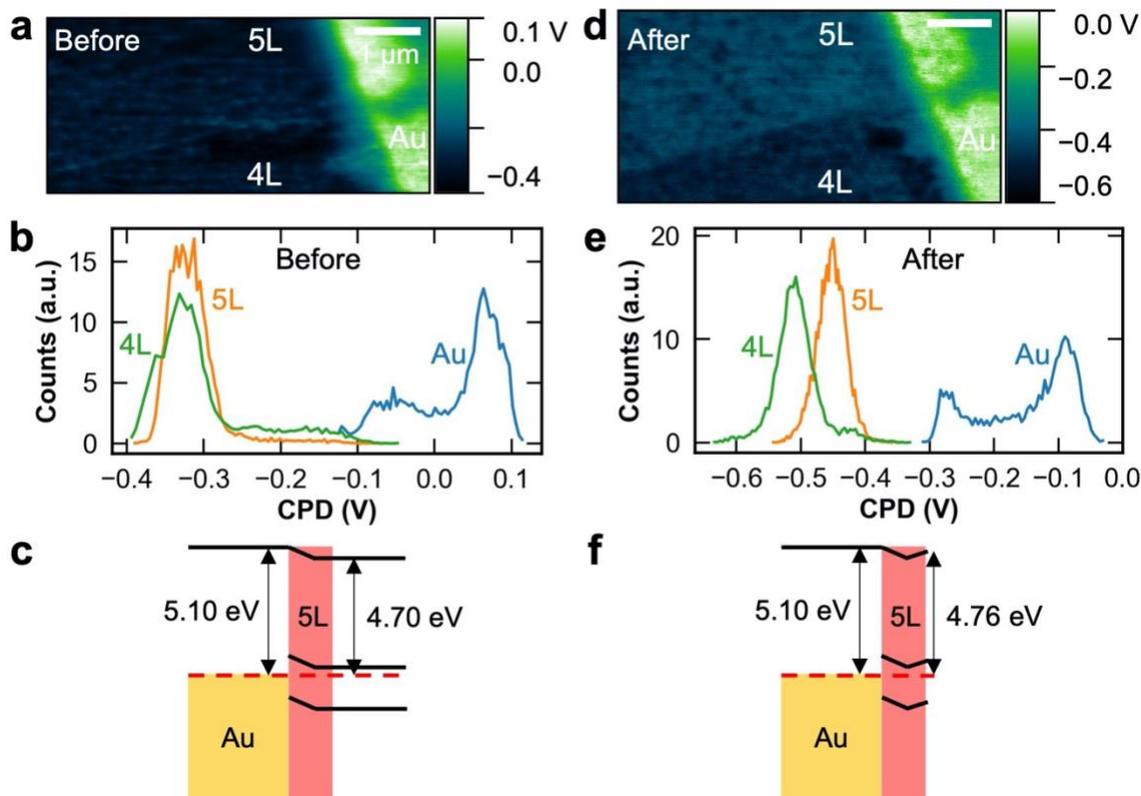
Figure 5.2. Change in surface potential after functionalization. KPFM (a) Contact potential difference (CPD) map, (b) CPD histogram, and (c) schematic band diagram of the 4L/5L MoS₂ on an Au substrate before functionalization. (d) CPD map, (e) CPD histogram, and (f) schematic band diagram after functionalization.

5.3. Development of Interlayers for Printed MoS₂ TFTs

Voids in printed vdW films may be filled by depositing an interlayer that physically and electronically bridges the 2D nanosheets.[28,74] A set of design principles must be followed towards designing such material. Firstly, the conduction band of the interlayer must be aligned with that of the 2D material to minimize the energetic barrier for charge transfer between the nanosheets. Secondly, the Fermi level of the interlayer must be optimized to ensure that the material is moderately conductive and non-degenerately dopes the 2D material. Thirdly, the density of

interfacial states between the interlayer and the 2D material must be minimized, preserving the vdW interface. Lastly, the interlayer must be processed at temperatures that are below the thermal budget of plastic substrates. To adhere to these principles, we explored the use of atomic layer deposition (ALD) of SnS_2 and SnO_x interlayers for printed MoS_2 TFTs. The low-temperature ALD processes are likely to allow for physisorptive nucleation without covalent bonding to the 2D material, thereby preserving the vdW structure and thus the electronic properties.[94,95]

5.3.1. ALD-Grown SnS_2 on Aerosol-Jet Printed MoS_2 TFTs

Within the SnS_x family, the conduction band of semiconducting SnS_2 is well aligned with that of MoS_2,[96,97] which should minimize the energetic barrier for charge transfer between MoS_2 nanosheets. To test this hypothesis, we used ALD (150 °C, Section 2.5.1) to grow SnS_2 on test SiO_2/Si substrates (Figure 5.3a) and directly on aerosol-jet printed MoS_2 films (Figure 5.3b) produced by the Hersam Group. The SnS_2 film grown on SiO_2 displayed a flat island morphology with a grain size of approximately 20 nm (Figure 5.3a), indicating c-axis orientation. Grazing incident wide-angle X-ray scattering (GIWAX, credit to Dr. Lee J. Richter at NIST) revealed that SnS_2 on printed MoS_2 is highly c-axis oriented with a mixed index diffraction series of (001) and (101) (Figure 5.3b). The (101) feature present in the SnS_2 film on printed MoS_2, which was not observed in the control films on native or thick oxides (Figure 5.3c,d), suggests that SnS_2 inherits the c-axis orientation of printed MoS_2. The coexistence of MoS_2 (002) and SnS_2 (001) also suggests that SnS_2 is c-axis oriented.
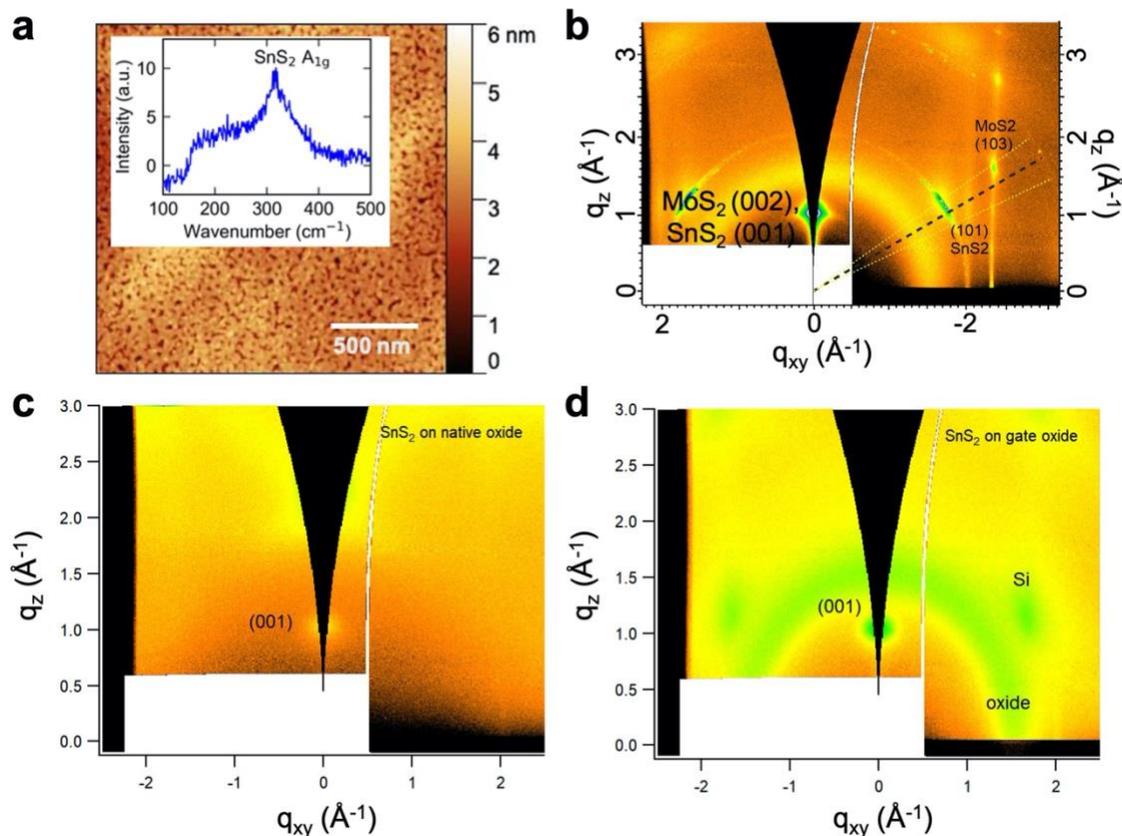
Figure 5.3. Structural characteristics of ALD SnS$_2$. (a) Representative AFM and Raman spectrum (inset) of 8 nm SnS$_2$ films grown by ALD (150 °C, 200 cycles, Section 2.5.1) on SiO$_2$/Si. Grazing incident wide-angle X-ray (GIWAX) scattering pattern of 8 nm SnS$_2$ on (b) 6 nm printed MoS$_2$, (c) Si substrate with native oxide, and (d) 285 nm SiO$_2$/Si substrate. The GIWAX was measured by Dr. Lee J. Richter from NIST. The thicknesses of SnS$_2$ and MoS$_2$ were determined using ellipsometry, also by Dr. Richter.

We investigated the effect of SnS$_2$ (100 cycles, 4 nm) on the conductivity of printed MoS$_2$ TFTs with varying thicknesses in collaboration with Sonal V. Rangnekar from the Hersam group. A thin film (<5 nm) with a low density of nanosheets contains voids that limit network percolation, leading to lower conductivity (Figure 5.4a). After SnS$_2$ deposition, both the on-state conductivity and the effective film mobility increased (Figure 5.4b,c), likely due to SnS$_2$ bridging the

nanosheets and increasing percolation for improved network transport. In contrast, a thicker and more densely packed film (~10 nm, Figure 5.4d) that is sufficiently percolative showed decreased conductivity and effective mobility after SnS_2 deposition (Figure 5.4e,f), which can be attributed to screening of the gate electric field by the semiconducting adlayer, resulting in decreased carrier concentration in the sheets. The SnS_2 may also intercalate between interconnected sheets and impede intersheet transport. As discussed in Chapter 3, for percolative films with planar stacking of nanosheets, transport is limited by nanosheet edges and gate screening rather than intersheet resistance and percolation. Therefore, the focus should be on passivating the edge states, exfoliating thin nanosheets, and printing thin, percolative films.[1]

We also show that the device performance of bottom-contacted devices is impacted by contact resistance (*i.e.*, the MoS_2 was printed on top of pre-patterned Au contacts). Figure 5.4e,f shows that the field-effect mobility increases with an increasing channel length, suggesting that contact resistance contributes to the underestimation of the field-effect mobility, especially for smaller channel lengths.[63] These findings led to a near-term focus on optimizing top contacts on printed MoS_2 film in collaboration with the Hersam group.
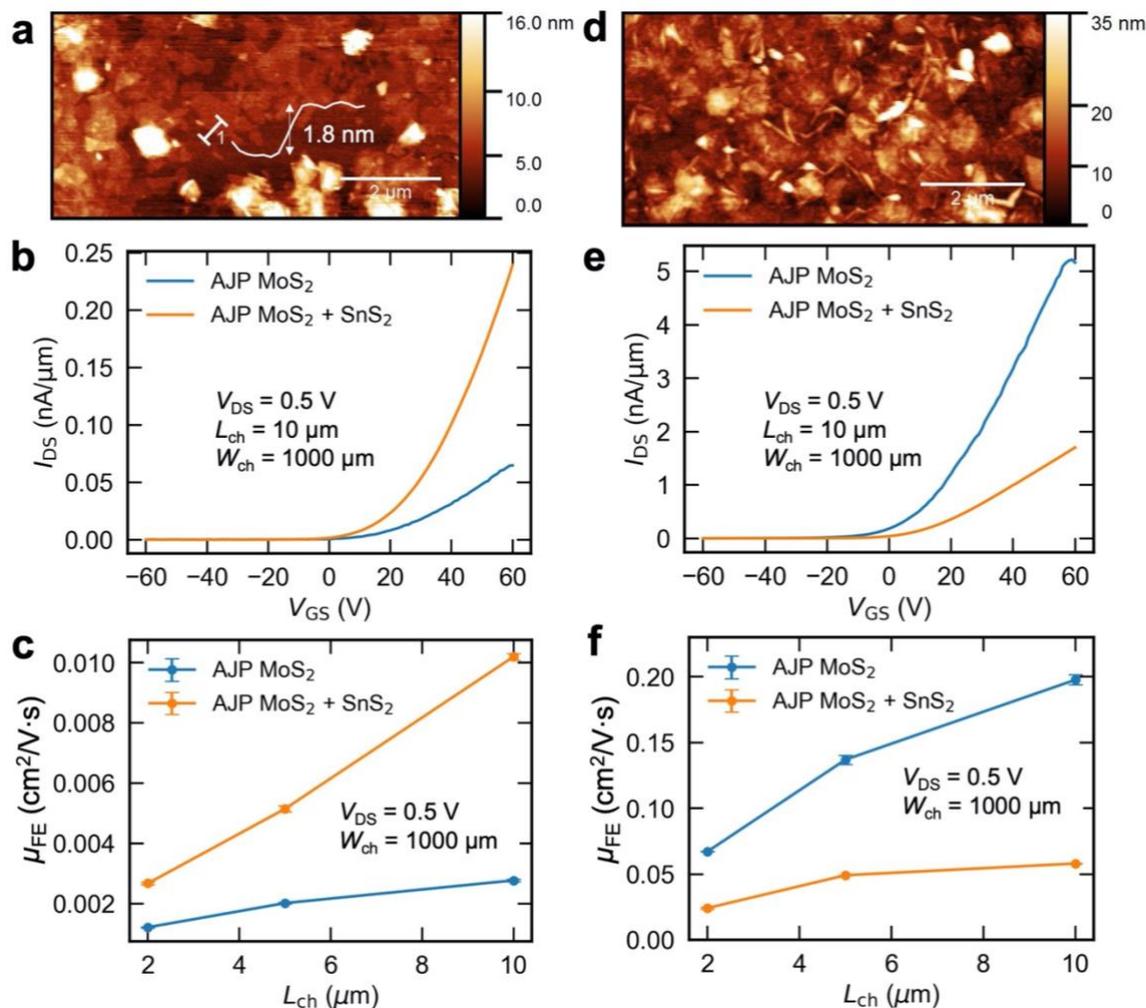
Figure 5.4. Influence of ALD SnS₂ on the field-effect characteristics of printed MoS₂ TFTs. AFM micrographs for representative (a) thin (<5 nm) and (d) thick (~10 nm) printed MoS₂ films. (b) drain-source current density I_{DS} vs. gate-source voltage V_{GS}, and (c) field-effect mobility μ_{FE} vs. channel length L_{ch} before (blue) and after (orange) ALD SnS₂ for film (a). (e) I_{DS} vs. V_{GS} and (f) μ_{FE} vs. L_{ch} before and after ALD SnS₂ for film (d). The error bars represent the standard error of the estimate from the Y-function analysis (Section 2.2). The nominal SnS₂ thickness is 4 nm (100 cycles). Channel width $W_{ch} = 1000$ μm for all devices. $V_{DS} = 0.5$ V for all transfer curves.

5.3.2. ALD-Grown SnO$_x$ in Model Systems

Moody et al. from the Lauhon Group have shown that introducing an ALD SnO$_x$ interlayer at the MoS$_2$/metal interface reduces the contact resistance.[86] This observation motivated us to investigate whether SnO$_x$ can also reduce the junction resistance between MoS$_2$ nanosheets. To test this hypothesis, we explored the influence of SnO$_x$ on the mobility and carrier concentration of MoS$_2$ using model systems.

During the ALD growth of SnO$_x$ (80 °C, Section 2.5.2), we performed in situ transport measurements on a few-layer MoS$_2$ FET using the experimental set-up developed by Moody and coworkers.[98] Transfer curves taken at interval growth cycles show a sharp conductivity increase and a negative threshold voltage shift in the first 10 growth cycles (Figure 5.5a). Y-function analysis (Section 2.2) was performed on the transfer curves to extract the field-effect mobility and change in carrier concentration at different growth stages (Figure 5.5b). In the initial stage, where the SnO$_x$ is less than 2 nm, both the mobility and carrier concentration increase sharply. Specifically, the mobility increases from 19.5 cm^2/V·s to 31.8 cm^2/V·s, and the carrier concentration increases by 1.6×10^{12} cm^{-2}. The improved mobility can be attributed to enhanced screening of charged impurities by the adlayer, as the increased permittivity relative to vacuum decreases the Coulomb potential of the charged impurities.[98] The increase in carrier concentration suggests that the Fermi level of SnO$_x$ is higher than that of MoS$_2$, leading to electron doping. The additional free carriers can further enhance screening of the charged impurities, thereby improving the mobility.
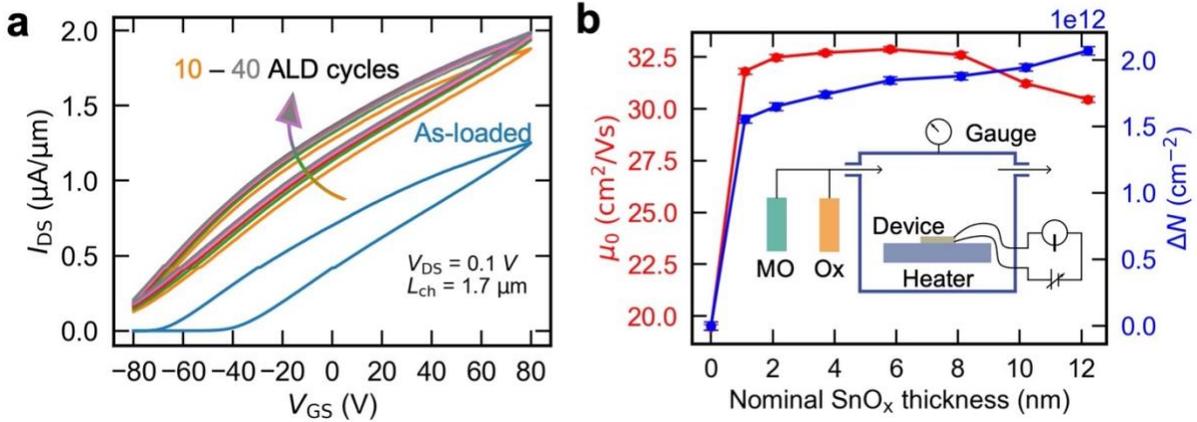
Figure 5.5. Influence of SnO$_x$ on the field-effect characteristics of a *single-crystal* MoS$_2$ FET. (a) I_{DS} vs. V_{GS} of a few-layer MoS$_2$ FET as-loaded and during interval ALD cycles of SnO$_x$. (b) Extracted low-field mobility μ_0 and change in carrier concentration ΔN vs. nominal SnO$_x$ thickness on MoS$_2$. $\Delta N = C_{ox} \times \Delta V_{th}$, where C_{ox} is the gate oxide capacitance and V_{th} is the threshold voltage extracted by the Y-function method (Section 2.2). The error bars represent the standard error of the estimate. The SnO$_x$ thickness was calculated by calibrating the QCM thickness with the thickness measured by AFM (Section 2.5.2). The inset shows a schematic of the experimental set-up for the *in situ* transport measurement.[98]

We then attempted to explore the influence of the SnO$_x$ interlayer on the junction resistance between MoS$_2$ nanosheets. We fabricated a model system (Figure 5.6a) comprising 3.9 nm SnO$_x$ sandwiched between mechanically exfoliated and transferred 6L-MoS$_2$ nanosheets (Figure 5.6b). The model system includes six distinct regions, allowing us to examine the impact of SnO$_x$ on both top and bottom nanosheets and the junction.

We performed Raman mapping on the model system to examine the influence on doping and strain based on shifts in characteristic A_{1g} and E_{2g} modes (Figure 5.6c,d):[99]

$$\begin{pmatrix} \Delta\omega_E \\ \Delta\omega_A \end{pmatrix} = \begin{pmatrix} -2\gamma_E\omega_0^E & k_n^E \\ -2\gamma_A\omega_0^A & k_n^A \end{pmatrix} \begin{pmatrix} \varepsilon \\ n \end{pmatrix}$$

(5.2)

where $\Delta\omega_E$ and $\Delta\omega_A$ are the peak positions shifts for E_{2g} and A_{1g}, ω_0^E and ω_0^A are the reference peak positions, γ_E, γ_A, k_n^E and k_n^A are the prefactors relating strain ε and doping n to the E_{2g} and A_{1g} shifts. The MoS$_2$ A_{1g} mode is strongly dependent on carrier concentration because the d_{z^2} orbital at the K point at the bottom of the conduction band has the same symmetry as the A_{1g} mode, thereby resulting in stronger electron-phonon coupling for the A_{1g}, where higher carrier concentration causes redshift and broadening of A_{1g}.[100] In contrast, the in-plane E_{2g} mode is mainly affected by uniaxial strain, where greater tensile strain causes a redshift of E_{2g}.[101]

We observed redshifts in both A_{1g} and E_{2g} peaks for the bottom MoS$_2$ with SnO$_x$ deposited on top (i.e., b-MoS$_2$/SnO$_x$), corresponding to more electron doping and compressive strain compared to the bottom MoS$_2$ on SiO$_2$ (Figure 5.6e).[99] The prefactors reported for MoS$_2$ (refs.[100,102]) were used to calculate an average increase in carrier concentration of $(1.82 \pm 0.95) \times 10^{12}$ cm^{-2} and an average strain of (-0.03 ± 0.02) %. The extracted carrier concentration from Raman mapping was consistent with that from analyzing the transfer curves (Figure 5.5b). In contrast, negligible peak shifts (Figure 5.6f) were observed for the top MoS$_2$ on SnO$_x$ compared to SiO$_2$, which can be attributed to the weaker interaction between the transferred nanosheet and the substrate. Indeed, the top MoS$_2$ on SiO$_2$ shows blueshifts (Figure 5.6e,f) and narrower peak widths (Figure 5.7) for the A_{1g} compared to the bottom MoS$_2$ on SiO$_2$, suggesting weaker electron-phonon due to n-doping from the substrate.[99,100] Although the junction shows a negligible A_{1g} peak shift with the sandwiched SnO$_x$ (Figure 5.6g), the A_{1g} peak broadens due to electron doping of the SnO$_x$ to the bottom MoS$_2$ (Figure 5.7). The above analysis demonstrates that Raman spectroscopy can be useful in probing spatial variations in doping and strain, potentially complementing electrical and KPFM measurements. Furthermore, the approach of using a two-nanosheet model system to

simulate behaviors in printed films was tested and later adopted to accomplish the published work

reported in Chapter 3.[1]
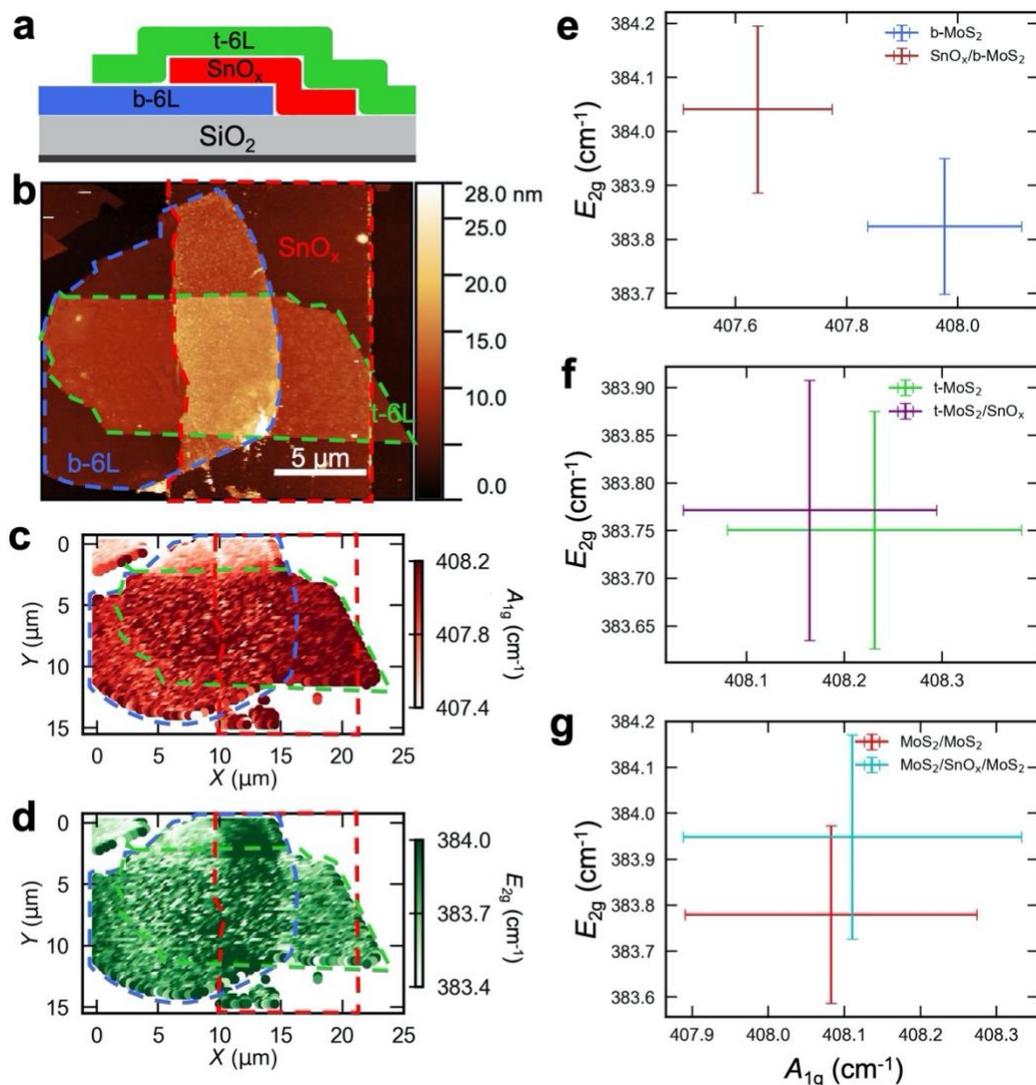
Figure 5.6. Influence of SnO_x in a $MoS_2/SnO_x/MoS_2$ model system. (a) Schematic and (b) AFM micrograph of a fabricated 6L-MoS_2/SnO_x/6L-MoS_2. The SnO_x is 3.9 nm. Raman maps of MoS_2 (c) A_{1g} and (d) E_{2g} peak positions. At each pixel, the spectra for MoS_2 and Si were fitted by Voigt functions with a linear background, and the extracted MoS_2 peak positions were calibrated by that of the Si. E_{2g} vs. A_{1g} peak positions for different regions: (e) b-MoS_2/SiO_2 and SnO_x/b-MoS_2/SiO_2, (f) t-MoS_2/SiO_2 and t-MoS_2/SnO_x, and (g) MoS_2/MoS_2/SiO_2 and MoS_2/SnO_x/MoS_2/SiO_2. The error bars represent one standard deviation from the mean value when sampling the peak positions in the region of interest.
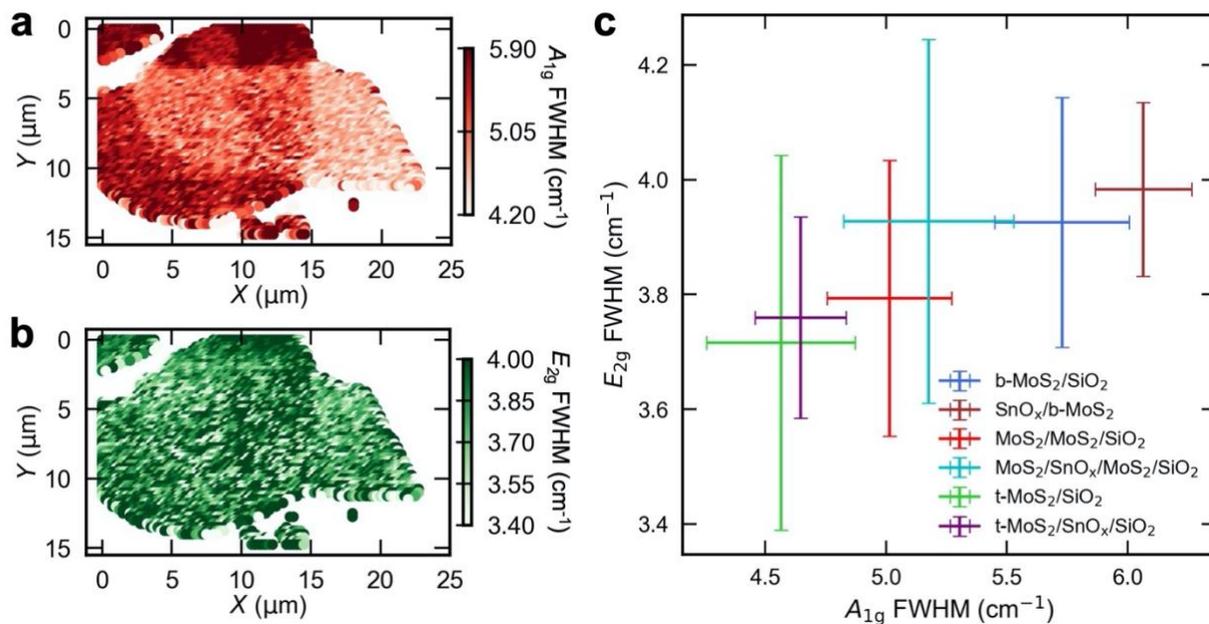
Figure 5.7. Raman peak width maps for the MoS₂/SnO$_x$/MoS₂ model system. Raman maps of MoS₂ (a) A_{1g} and (b) E_{2g} FWHM. (c) E_{2g} vs. A_{1g} FWHM for different regions. At each pixel, the spectra for MoS₂ and Si were fitted by Voigt functions with a linear background. The error bars represent one standard deviation from the mean value when sampling the peak widths in the region of interest.

5.4. Conclusion

In summary, we explored various strategies to improve the performance of printed MoS_2 TFTs. We attempted edge functionalization of MoS_2 using molecules containing a 1,2-dithiolane group, which was predicted to covalently bind to sulfur vacancies but observed deposition on both edges and the basal plane. This outcome prompted further investigation into designing molecules with distinct interactions between edge sites and the basal plane. Moreover, we examined the development of ALD interlayer materials that could physically and electronically bridge 2D nanosheets and fill voids in printed vdW films. Our findings showed that ALD SnS_2 improves the on-state conductivity and field-effect mobility in printed MoS_2 channels with a low nanosheet density but decreases the performance of sufficiently percolative channels. These observations emphasize the advantages of passivating edge states, exfoliating thin nanosheets, and printing thin, percolative films. Additionally, we investigated the impact of ALD SnO in model systems, including a single-sheet MoS_2 FET and a MoS_2/SnO/MoS_2 sandwich structure, through *in situ* transport measurements and Raman spectroscopy. This research ultimately led to the published work reported in Chapter 3.[1]

Chapter 6   Exploring Non-Volatile Memory in Mixed Ionic-Electronic TFTs

6.1.   Introduction

Integrating non-volatile memory into TFTs is a promising avenue to expand the capabilities of emerging printed circuit technologies. Logic-in-memory computing, also known as memory-based computing or in-memory computing, is a computing architecture where data storage and processing occur within the same physical device. This architecture differs from conventional circuits, which separate memory and processing units, necessitating data transfer between them for computation. Logic-in-memory computing provides advantages such as accelerated data transfer, reduced energy consumption, and enhanced performance for parallel tasks, laying the groundwork for novel computing paradigms like neuromorphic computing.

To enable non-volatile memory in transistors, researchers have been exploring the integration of photoswitches (*i.e.*, photoswitchable molecules).[103–126] Photoswitches, also known as photochromic molecules, are a class of chemical compounds that exhibit reversible changes in their molecular structure, absorption properties, and electronic states upon exposure to specific wavelengths of light. The process involves a photoinduced transformation between two distinct isomeric forms, typically in response to ultraviolet (UV) and visible light. Each isomeric form possesses a unique dipole moment, allowing for optical modulation of non-volatile memory in transistors. Section 6.2 summarizes results from a literature survey on photoswitch-modulated FETs, aiming to elucidate the performance limitations in existing devices in terms of modulation magnitude and timescale, and to identify underexplored design concepts. Section 6.3 presents proof-of-concept device demonstrations that utilize the photoswitchable ion-binding properties of

spiropyran to explore whether this property can modulate the electrical characteristics of electrochemical transistors (Section 6.3.1) and electrolyte-gated transistors (Section 6.3.2).

6.2. Literature Survey on Photoswitch-Modulated FETs

The literature survey on photoswitch-modulated devices aims to answer the following questions:

1. What device concepts have been explored, and what novel functions have been achieved?

2. Which device components have photoswitches been integrated with? What are the magnitude and timescale of modulation, and what are the mechanisms?

3. What factors limit the performance of existing photoswitch-modulated devices? How can these limitations be overcome by novel materials, heterostructures, and devices?

To efficiently survey this research area, ResearchRabbit, an AI-based open-access tool, was employed. This tool allows researchers to compile and sort research papers while also *exploring relevant papers and authors* within the same interface. Given initial starting papers, the tool automatically identifies relevant papers based on title, author list, and abstract, and generates both network and timeline representations of highly relevant papers, with more recent papers appearing darker in color (Figure 6.1). The tool can also generate a shareable link to a collection of papers (*e.g.*, Photoswitch-Modulated-Devices_ZZ), facilitating communication between collaborators.

The survey reveals that photoswitches have been predominantly utilized to modulate the electrical characteristics of organic FETs. The Paolo Samori (University of Strasbourg, France), Xuefeng Guo (Peking University, China), and Yutaka Wakayama (National Institute for Materials Science, Japan) groups appear to be at the forefront, consistently publishing relevant papers over

many years. Representative papers from these groups were subsequently selected for a comprehensive review.
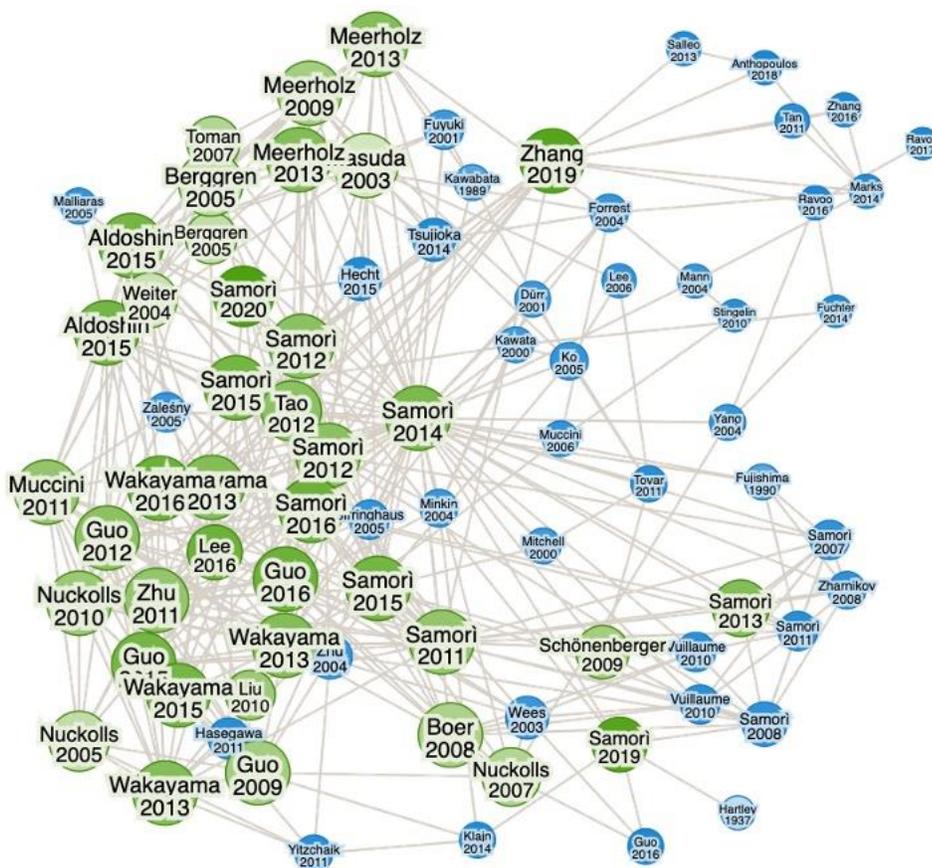
Figure 6.1. Network representation of relevant papers for photoswitch-modulated devices. Link to the collection of papers: Photoswitch-Modulated-Devices_ZZ.

6.2.1. Photoisomerization of Common Photoswitches Used in FETs

Common photoswitches utilized in FETs include azobenzene, diarylethene, and spiropyran (Figure 6.2). Azobenzene (AZO) undergoes isomerization from its trans to cis configuration upon exposure to UV light, while visible light reverts it back to the trans form. The trans form has a

planar structure with a negligible dipole moment, whereas the non-planar, bent cis form exhibits a dipole moment of approximately 3 Debye.[127] Diarylethene (DAE) molecules undergo reversible photoisomerization between open-ring and closed-ring forms upon exposure to UV and visible light, respectively. The closed-ring form, which forms a single bond between the two aryl rings, has a dipole moment of approximately 4 Debye.[128] Additionally, the closed-ring form exhibits a higher highest occupied molecule orbital (HOMO) and a lower lowest unoccupied molecular orbital (LUMO) compared to the open-ring form.[104,121] Spiropyran (SP) experiences reversible photoisomerization between closed-ring and open-ring forms upon exposure to UV and visible light, respectively. The closed-ring SP form has a non-planar structure and a dipole moment of 6 Debye, while the open-ring merocyanine (MC) form has a planar structure with spatially separated charged sites, leading to an increased dipole moment of 14 Debye.[129] These charged sites in the MC form can function as ion-binding centers,[130] enabling the modulation of free ion concentration with light (Section 6.3).
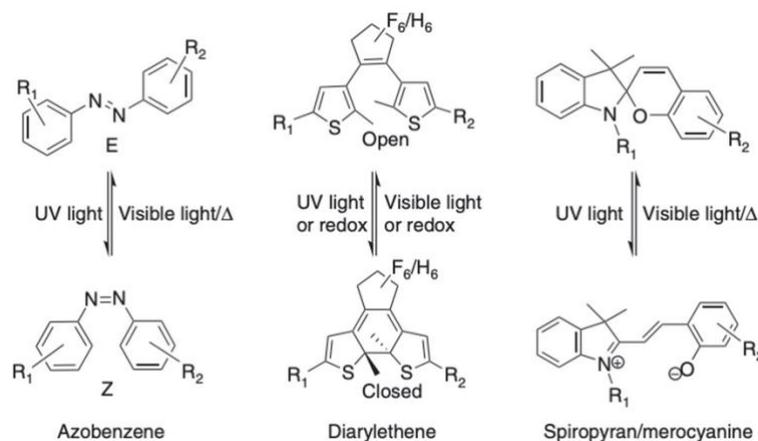
Figure 6.2. Photoisomerization of azobenzene, diarylethene, and spiropyran. Reprinted with permission from Springer Nature.[131]

6.2.2. Photoswitch-Functionalized FET Components, Switching Conditions, and Optically Modulated Performance

This spreadsheet (Photoswitch-Modulated_Devices.xlsx) provides a summary of FET components functionalized with photoswitches, switching conditions (including switching time and operating voltage), optically modulated performance, and proposed mechanisms in 24 representative papers.

Incorporating memory in FETs has been achieved through various approaches, such as depositing self-assembled monolayers (SAMs) at the channel/contact interface,[103,104,115] blending photoswitches with the channel,[105,106,120–126] depositing a thin layer on the channel[107–109] or at the channel/dielectric interface,[110–113] and utilizing photoswitches as dielectrics[114,116] or semiconducting channels.[117–119] Samori and colleagues demonstrated an optically modulated organic TFT functionalized with a SAM of DAE molecules at the metal/semiconductor interface.[104] The device exhibited approximately 70% increases in both drain-source current and mobility upon 10 minutes of UV light irradiation. This increase was attributed to the lower LUMO of the closed-ring DAE, which consequently reduces the metal/semiconductor tunneling barrier. The same group also explored blending photoswitches with organic channels, which can trap or de-trap charge carriers based on energy level differences between the photoswitch isomers and the organic semiconductor.[121] A DAE-functionalized P3HT device demonstrated a 90% current increase with 15 seconds of UV irradiation.[124] The authors claimed that the higher HOMO of the closed-ring DAE facilitates hole transport from P3HT to DAE, thus increasing the device conductance through photoisomerization. Moreover, photoswitches can modulate carrier

concentration in the channel via changes in dipolar doping. Guo and coworkers reported depositing SP photoswitches as SAMs at the interface between a pentacene channel and SiO_2 dielectric, achieving 2× current modulation (*i.e.*, 100% current increase) with 15 minutes of UV irradiation.[111] This group also presented a SP-PMMA composite dielectric for pentacene TFTs, obtaining a 3× current modulation with 20 minutes of UV irradiation.[116] The most significant modulation, reported by the Samori group, involved depositing AZO-functionalized CoPc molecules on a MoS_2 FET, resulting in a 10× current modulation with 1 minute of UV irradiation.[109] Furthermore, the Wakayama group has published several papers on using photoswitches as channels. Although these devices demonstrated large current modulations (100-1000×), the mobility of photoswitches is typically very low (10^{-5} $cm^2V^{-1}s^{-1}$) and far inferior to that of semiconducting polymers and 2D materials.[117–119]

6.2.3. Performance Limitations and White Space

The literature survey presented above reveals that despite achieving large current modulations, the switching times for these devices range from tens of seconds to minutes. This duration is impractical for their application as elements in printed integrated circuits. A commonly accepted explanation for the slow switching in solid-state is the volume change associated with photo-isomerization.[132] In the solid state, steric hindrance impedes the necessary conformational change, leading to slower switching compared to that in solution.

To achieve both large modulation and ultrafast switching simultaneously, several research directions can be pursued. Firstly, the development of faster photoswitches in solid-state can be explored, such as photoswitchable polyelectrolytes where the photoswitches are spatially separated.[133,134] Secondly, devices with more responsive channel materials, like 2D materials,

could be investigated because the device responses are typically more sensitive to changes in contacts and dielectrics compared to organic FETs.[108,109] Thirdly, the ion-binding property of photoswitches, like spiropyran/merocyanine, can be leveraged in mixed ionic-electronic transistors, such as electrochemical transistors and electrolyte-gated transistors, to achieve optical control over ionic-electronic transport. The presence of ions can also modulate the switching of photoswitches, enabling electrical control of photoswitching. This bimodal modulation of switching could significantly improve the switching speed. For instance, ref.[113] demonstrated the use of spiropyran salts as the dielectric for fullerene TFTs, achieving $10^4\times$ current modulations and microsecond photoswitching when a gate-source voltage is applied.

6.3. Proof-of-Concept Device Demonstrations of Photoswitchable Ion-Binding

The ion-binding property of spiropyran has been demonstrated in various systems such as solutions,[135,136] polymer electrolytes,[137] polyelectrolytes,[133,134] and inorganic hosts (*e.g.*, carbon nanotubes)[138] for modulating ionic conduction and sensing metals. To leverage this property for building memory in transistors, we devised two approaches. The first approach involves introducing spiropyran into the electrolyte to modulate the free ion concentration via photoisomerization, which could potentially change the volumetric capacitance for electrochemical transistors and/or the electric double-layer capacitance for electrolyte-gated transistors. The second approach involves functionalizing the bulk semiconducting channel in electrochemical transistors with spiropyran so that photoisomerization can trap ions injected from the electrolyte, thereby modulating the device conductance and hysteresis.[139] Considering that the second approach requires developing new composites and processes, we explored the first approach, with the preliminary results documented in the following sections.

6.3.1. Incorporating Spiropyran in Electrochemical Transistors

In electrochemical transistors (ECTs), the applied gate-source voltage (V_{GS}) leads to the injection of ions from the electrolyte into the semiconducting channel, causing changes in the doping state throughout the channel volume. Hence, the transconductance g_m of ECTs is characterized by the volumetric capacitance:[140]

$$g_\mathrm{m} = \frac{W}{L} d C^* \mu (V_\mathrm{TH} - V_\mathrm{GS})$$

(6.1)

where W, L, and d are the channel width, length, and thickness, respectively, C^* is the capacitance per unit volume, μ is the mobility, and V_TH is the threshold voltage.

Rivnay and colleagues demonstrated that by engineering the microstructure of a polymer composite, ions can be trapped in the channel to create non-volatile memory.[139] We were interested in exploring whether trapping ions in the electrolyte through the photoisomerization of spiropyran to merocyanine could create optically modulated non-volatile memory. To test this hypothesis, we examined spiropyran-containing electrolytes in a typical PEDOT:PSS organic electrochemical transistor (OECT), collaborating with Dr. Xudong Ji from the Rivnay Group at Northwestern University.

The experimental setup was similar to that shown in Figure 2.18, but with an OECT instead of an electrolyte-gated transistor. Figure 6.3a,b shows the typical output and transfer curves of a PEDOT:PSS OECT in an 0.1 M aqueous NaCl solution. The device operates as a p-type depletion-mode transistor. The negatively charged -SO_3^- group in PSS induces free holes in the PEDOT chain, resulting in hole conductivity at $V_\mathrm{GS} = 0$ V. As positive V_GS is applied, cations compensate the charges on the -SO_3^- group in PSS, which reduces the free hole concentration and consequently lowers the conductivity.

The same device was then measured in 50 mM $ZnCl_2$ in ethyl acetate, a solvent used to dissolve $ZnCl_2$ and spiropyran because spiropyran and various other photoswitches have aromatic groups that render them intrinsically hydrophobic. The device exhibited increased conductivity with minimal gate modulation (Figure 6.3c,d), suggesting that an insufficient number of ions penetrated the channel to decrease the hole concentration. Introducing a small amount of water (20 μL) to the nonaqueous electrolyte (200 μL) improved gate modulation (Figure 6.3e,f), implying that water is essential for ion transport within the polymer channel. Indeed, previous reports suggest that water plasticizes the polymer chain to enhance chain motion and solvates the ions to enable ionic transport in the polymer.[141] Therefore, the photoswitches must be water-soluble to interact with solvated ions that penetrate into the semiconductor volume. The transfer curves measured in the cosolvent exhibited increased hysteresis compared to the aqueous NaCl solution (Figure 6.3f), which can be attributed to the slow diffusion of ions from ethyl acetate to H_2O for gating the channel.

Future research in this area may include developing water-soluble photoswitches, which could involve functionalizing the molecules with charged, water-soluble groups like $-SO_3^-$.[142] However, if both the ions and the photoswitches are strongly solvated by water molecules forming hydrogen-bonded cages, the electrostatic interactions between the ions and photoswitches might be too weak for effective binding. Another direction involves creating a photoswitchable ionic liquid. In such a photoswitchable ionic liquid, where either the cation or anion could be a photoswitch derivative, photoisomerization may alter the electrostatic interaction between counterions, thus changing the ionic mobility and the RC time constant. Segalman and colleagues synthesized a DAE-based photoswitchable ionic liquid and demonstrated the modulation of ionic conductivity with UV/vis

irradiation.[143,144] If a photoswitchable ionic liquid is used to gate an ECT, the timescale of gate modulation could be altered with light, creating hysteresis and thus non-volatile memory.
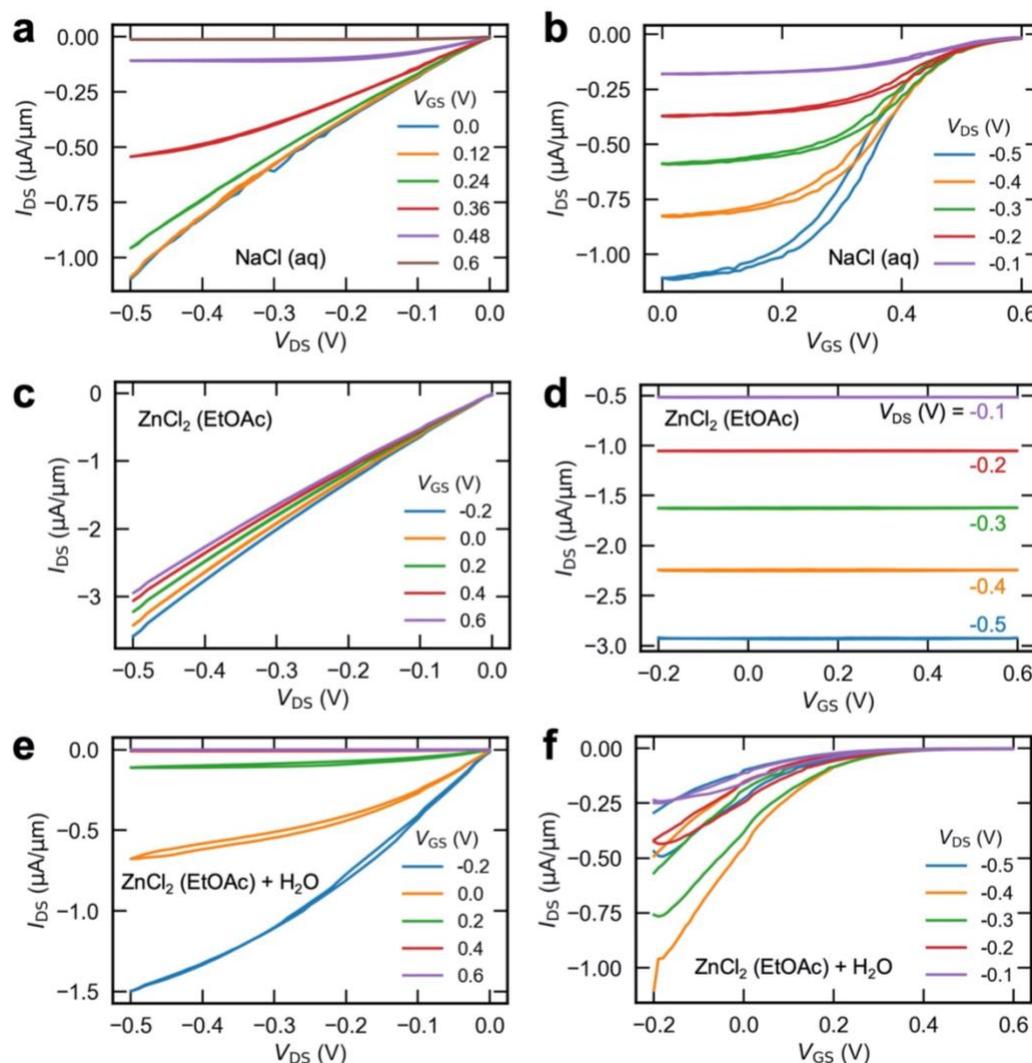
Figure 6.3. Electrical characteristics of a PEDOT:PSS electrochemical transistor in different electrolytes. (a) Drain-source current I_{DS} vs. drain-source voltage V_{DS} (*i.e.*, output curves) and (b) I_{DS} vs. gate-source voltage V_{GS} (*i.e.*, transfer curves) in 0.1 M aqueous NaCl solution. (c) Output and (d) transfer curves in 0.05 M $ZnCl_2$ in ethyl acetate (EtOAc) solution. (e) Output and (f) transfer curves in 200 μL 0.05 M $ZnCl_2$ (ethyl acetate) with 20 μL H_2O. The channel length, width, and thickness are 10 μm, 100 μm, and 100 nm, respectively.

6.3.2. Incorporating Spiropyran in Electrolyte-Gated Transistors

The conductance of electrolyte-gated transistors (EGTs) is influenced by the electric double-layer (EDL) capacitance, which arises at the interface between a conductive surface and an electrolyte. When a voltage is applied, ions from the electrolyte accumulate near the electrode via electrostatic adsorption and diffusion, forming the first layer, while an opposing charge layer develops within the electrode.[145] Within the electric double layer, solvent molecules become polarized, generating the EDL capacitance. The EDL capacitance can potentially be modulated by incorporating photoswitches to control the free ion concentration. To test this hypothesis, CVD-MoS_2 EGTs were fabricated (Figure 6.4, methods in Chapter 2 Section 2.6.2) and measured in spiropyran-containing electrolytes under UV irradiation (experimental set-up in Chapter 2 Section 2.6.2, Figure 2.18).
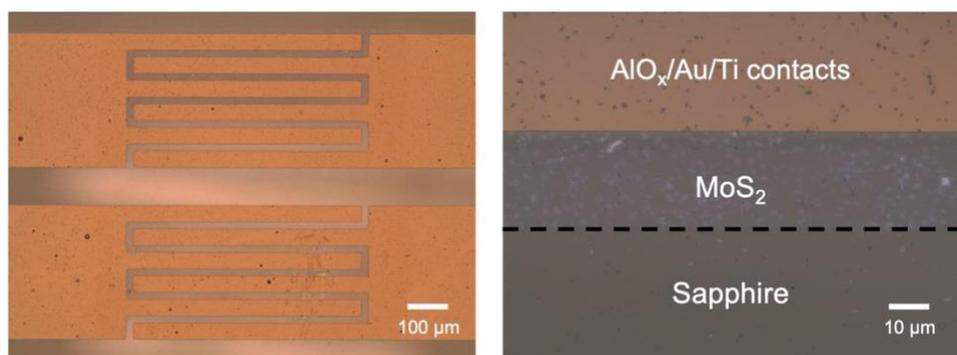
Figure 6.4. Optical micrographs of the CVD-MoS₂ electrolyte-gated transistors (EGTs) on a sapphire substrate with AlOₓ-encapsulated Au/Ti contacts.

Output and transfer curves of the device were measured in dark conditions in acetonitrile (Figure 6.5a,b) and electrolytes containing $ZnCl_2$ (Figure 6.5c,d) and $ZnCl_2$-SP mixture (Figure 6.5e,f). The device exhibited asymmetric output curves with higher conductance at negative V_{DS} even when the gate electrode is grounded (Figure 6.5a). This behavior indicates that the field between the drain and gate electrodes is sufficient to polarize the solvent molecules and cause subsequent accumulation of free electrons in MoS_2. The negative differential transconductance observed in the transfer curves (Figure 6.5b) could be due to trapping of solvent molecules or ions occurring slowly compared to the gate sweep rate.[146]
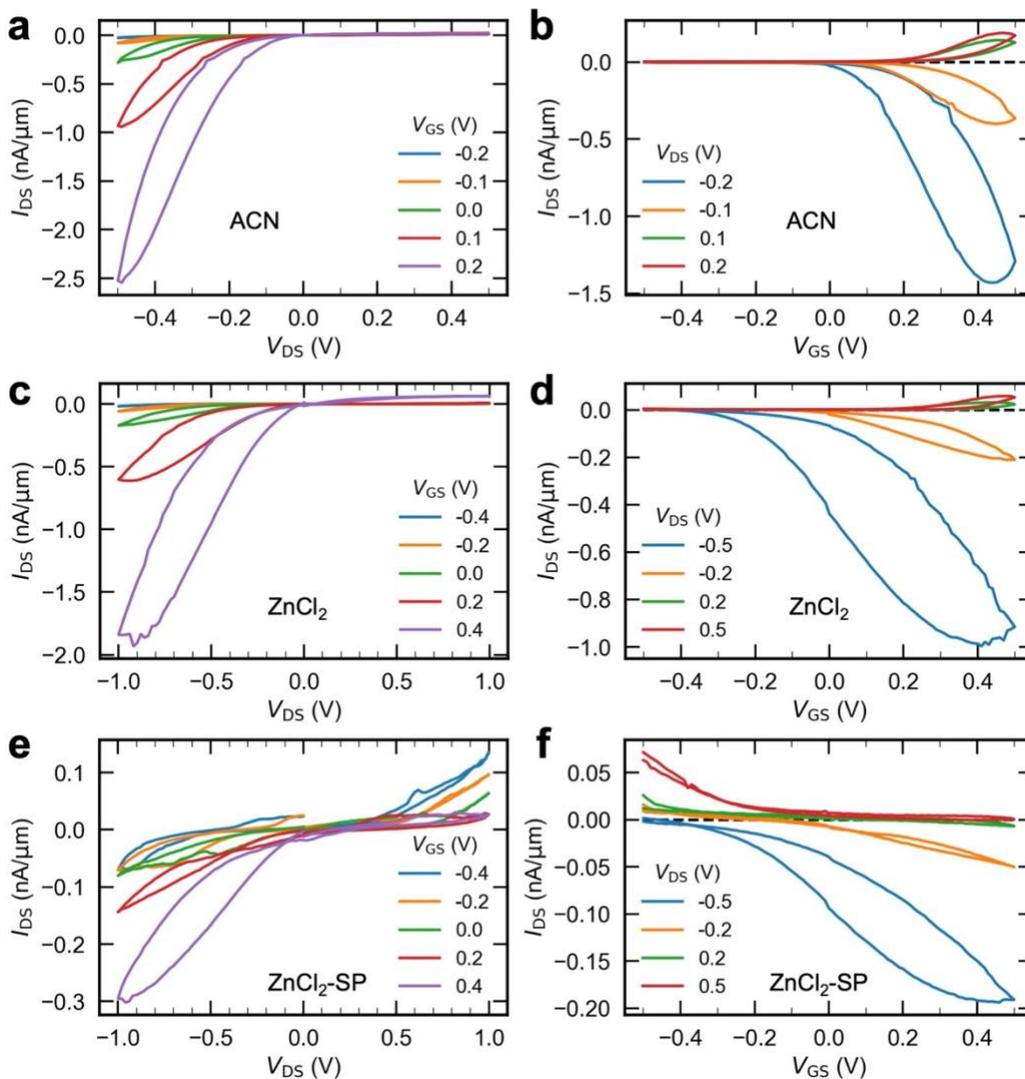
Figure 6.5. Electrical characteristics of CVD-MoS$_2$ electrolyte-gated transistors (EGTs). (a) Output and (b) transfer curves of an EGT measured in acetonitrile (ACN). (c) Output and (d) transfer curves of an EGT measured in 10 mM ZnCl$_2$. (e) Output and (f) transfer curves of an EGT measured in 10 mM ZnCl$_2$ and 40 mM spiropyran (SP). All were measured in dark before UV irradiation. The channel length is 20 μm. The sweep rates for V_{DS} and V_{GS} are 5 V/s and 10 V/s, respectively.

Current-time measurements were performed with chopped UV light in a dry condition (Figure 6.6a), in acetonitrile (Figure 6.6b) and electrolytes containing $ZnCl_2$ (Figure 6.6c) and $ZnCl_2$-SP mixture (Figure 6.6d). The device exhibited a gradual increase in photocurrent and significant persistent photoconductivity in response to UV irradiation (Figure 6.6a). These characteristics have been attributed to trapped charges in the substrate[147], adsorbates,[148] and the spatial separation of electron and hole traps,[149] resulting in an extended recombination time. In liquid environments, the dark current increased by $\sim100\times$, likely due to the slow diffusion of solvent molecules and/or ions to the MoS_2 surface, inducing more free carriers. This diffusion process, typically slower than electrostatic adsorption for double-layer formation, may not contribute to EDL capacitance during fast voltage sweeps. Indeed, output and transfer curves measured after the current-time experiment show comparable device conductance to that before the measurement (Figure 6.7). Contrary to our expectation that the UV-induced photoisomerization of SP to MC may capture ions, *reducing* the EDL capacitance and thus the free carrier concentration, the device conductance shows comparable percentage *increases* upon UV irradiation in both $ZnCl_2$ and $ZnCl_2$-SP electrolytes (Figure 6.6c,d left panels), which are attributed to the generation of excess free carriers. The photocurrent rise time in electrolytes is shorter than in pure acetonitrile, suggesting reduced trapping of free carriers, which is possibly due to ions chemisorbing at MoS_2 defects that passivate trap states (*e.g.*, anions binding to positively charged sulfur vacancies)

Our experiments did not provide evidence of EDL capacitance modulation through photoswitchable ion-binding. As mentioned earlier, the electrostatic interaction between solvated ions and photoswitches could be weakened due to the screening by solvent molecules. Future

research could explore the synthesis of photoswitchable ionic liquids to modulate volumetric capacitance in electrochemical transistors.
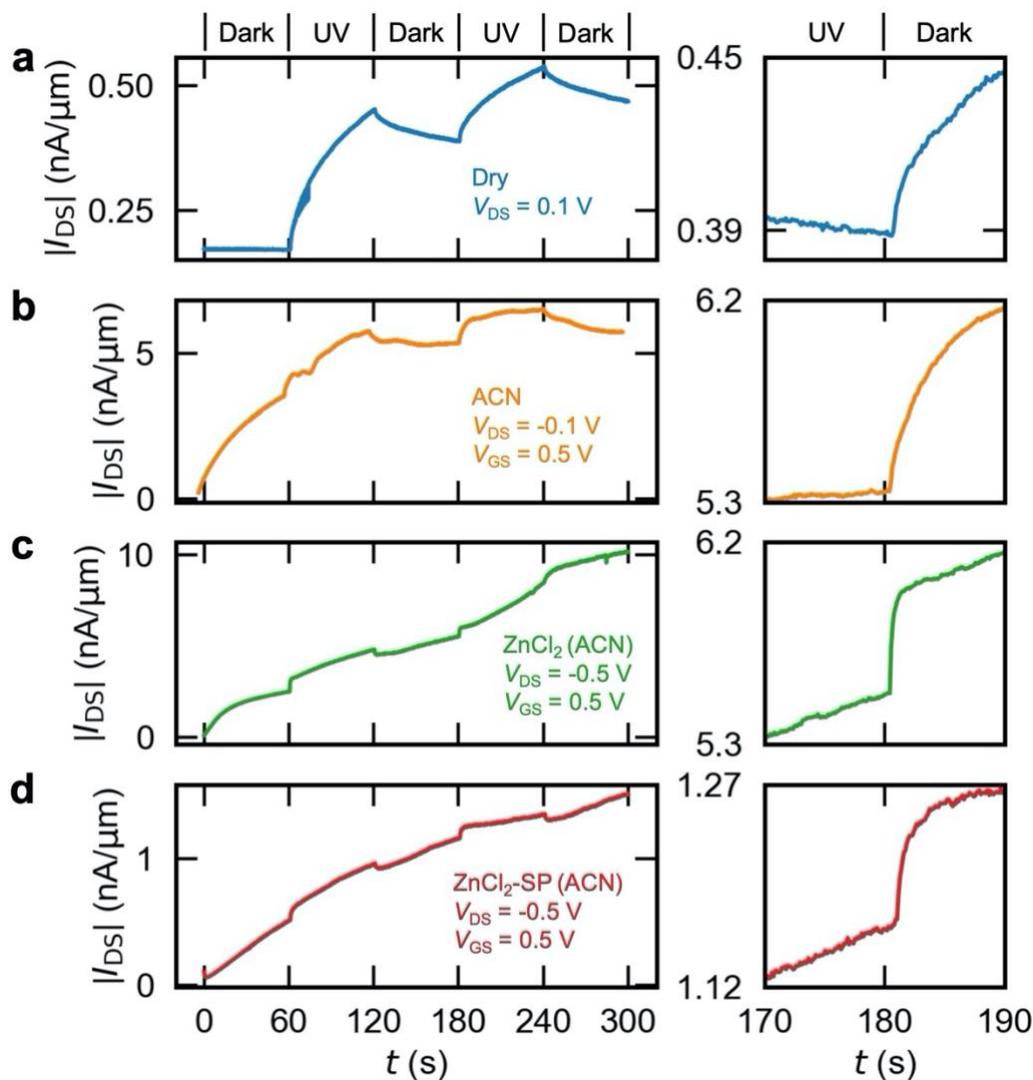
Figure 6.6. Evolution of CVD-MoS₂ EGT conductance with time and irradiation in different environments. Absolute drain-source current density |I_{DS}| vs. time (t) of the device in (a) dry condition, (b) acetonitrile (ACN), (c) 10 mM ZnCl₂ in ACN, and (d) ACN electrolyte of 10 mM ZnCl₂ and 40 mM spiropyran (SP) under chopped UV irradiation. The channel length is 20 μm.
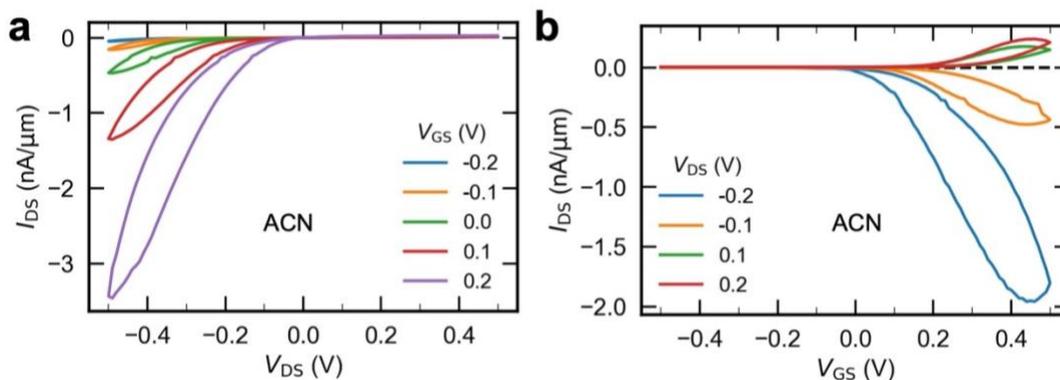
Figure 6.7. (a) Output and (b) transfer curves of the CVD-MoS$_2$ EGT in ACN after the current-time measurement. The channel length is 20 μm. The sweep rates for V_{DS} and V_{GS} are 5 V/s and 10 V/s, respectively.

6.4. Conclusion

In summary, we performed an extensive literature review on photoswitch-modulated devices and conducted preliminary experiments to investigate the feasibility of using spiropyran's photoswitchable ion-binding property to create memory in transistors. The literature review discussed FET components with photoswitches, switching conditions, and optically modulated performance, highlighting the slow switching that is likely caused by steric hindrance obstructing conformational changes in the solid state. This analysis points to future directions, such as designing polyelectrolytes with spatially separated photoswitchable groups, integrating photoswitches with atomically thin materials, and utilizing the ion-binding property of specific photoswitches. We attempted to incorporate spiropyran into electrolytes for organic electrochemical transistors and CVD-MoS$_2$ electrolyte-gated transistors but did not find evidence of capacitance modulation through photoswitchable ion-binding. Hence, we proposed a future direction involving the development of photoswitchable ionic liquids.

Chapter 7   Conclusions and Outlook

7.1.   Thesis Summary

This thesis has presented approaches in modeling, imaging, and processing aimed at optimizing the performance of printed vdW thin-film devices, such as transistors and photodetectors, as well as exploring the integration of non-volatile memory in TFTs with mixed ionic-electronic transport.

In Chapter 3, we developed and calibrated a resistor network model to analyze how near-edge and intersheet resistances influence the performance of printed 2D transistors as a function of nanosheet stacking, thickness, size, and density. For mechanically exfoliated MoS_2, the presence of fixed negative charges at nanosheet edges was shown to induce a large local increase in resistance that limits the effective mobility. When transport in the 2D film is limited by the near-edge resistance of high-mobility and moderately doped nanosheets, rather than the intersheet resistance, there is an optimum nanosheet thickness that can be targeted by exfoliation processes. Successful passivation of edges will enable the realization of higher mobilities with thinner nanosheets due to reduced junction resistances and reduced screening of the gate. For a film assembled from nanosheets that have lower mobility but higher dopant concentration, reducing the nanosheet thickness via development in exfoliation and sorting processes will improve both effective mobility and on/off ratio.

In Chapter 4, we characterized the topography of printed MoS_2 photodetectors using optical microscopy-based methods and verified the photoconductive behavior through local photoimpedance spectroscopy. Raman profiling of the polyimide substrate identified the contact locations, confirming that the photoresponse primarily originates from the MoS_2 channel. White

light interferometry revealed that the inhomogeneous photoresponse in the MoS_2 channel is due to thickness variations, which are likely caused by the photonic annealing method. Local photoimpedance measurements at the contacts showed negligible capacitance between the graphene contacts and the MoS_2 channel, confirming the formation of an ohmic junction, which contributes to the enhanced photoresponsivity of the photonically annealed devices.

In Chapter 5, we explored various strategies to improve the performance of printed MoS_2 TFTs. We attempted edge functionalization of MoS_2 using molecules containing a 1,2-dithiolane group but observed deposition on both edges and the basal plane. This outcome motivated further investigation into designing molecules with distinct interactions between edge sites and the basal plane. In addition, we examined the development of ALD interlayer materials that could physically and electronically bridge 2D nanosheets and fill voids in printed vdW films. We showed that ALD SnS_2 improves the on-state conductivity and field-effect mobility in printed MoS_2 channels with a low nanosheet density but decreases the performance of sufficiently percolative channels. This observation emphasizes the advantages of passivating edge states, exfoliating thin nanosheets, and printing thin, percolative films. Finally, we investigated the impact of ALD SnO in model systems, including a single-sheet MoS_2 FET and a MoS_2/SnO/MoS_2 sandwich structure, through *in situ* transport measurements and Raman spectroscopy. This research informed the work reported in Chapter 3.

Chapter 6 presented a comprehensive literature review on photoswitch-modulated devices and described preliminary experiments to explore the potential of utilizing the photoswitchable ion-binding property of spiropyran for creating memory in transistors. The literature review summarized FET components functionalized with photoswitches, switching conditions, and

optically modulated performance, and observed that the slow switching is likely caused by steric hindrance impeding conformational changes in the solid state. This analysis suggests future research directions including designing polyelectrolytes with spatially separated photoswitchable groups, incorporating photoswitches with atomically thin materials, and harnessing the ion-binding property of specific photoswitches. Schemes were explored for incorporating spiropyran into electrolytes that gate devices, including organic electrochemical transistors and CVD-MoS_2 electrolyte-gated transistors; however, we did not observe capacitance modulation through photoswitchable ion-binding. As a result, we proposed an alternative direction focused on developing photoswitchable ionic liquids.

7.2. Future Directions

Two research directions for printed vdW devices are given context by this thesis work. The first direction involves improving the performance of printed vdW optoelectronics by developing edge-selective functionalization approaches (Section 7.2.1). The second direction aims to broaden the functionalities of 2D inks by investigating novel device concepts, such as creating printed optically tunable capacitors (Section 7.2.2) and integrating memory with printed transistors (Section 7.2.3).

7.2.1. Edge Functionalization for Printed vdW Optoelectronics

As discussed in Chapter 3 and Chapter 5, developing edge-selective functionalization could enable the optimization of printed vdW TFT performance to compete with oxide TFTs. Functional molecules must be designed to exhibit distinct interactions with edge sites and the basal plane. For example, a chemically reactive functional group could be attached to a long, non-polar chain (*e.g.*, alkyl).[83] Moreover, it is crucial to consider that the chemistry and electronic properties at the edges

of 2D materials are dependent on crystal termination and environment. In MoS_2, the armchair edge is semiconducting and typically causes electron depletion in the adjacent basal plane, while the zigzag edge is metallic and usually leads to electron accumulation.[41,150–152] Oxidation of MoS_2 edges is expected under ambient conditions,[67–70] necessitating the development of a mild reducing agent to passivate edge states and locally increase electron concentration.[83]

Collaborative efforts to develop novel edge functionalization chemistry should be informed by characterizations that correlate edge chemistry and related properties with the junction characteristics of overlapping nanosheets influenced by the functional molecules. Tip-enhanced Raman spectroscopy can be employed to determine edge structure (*i.e.*, zigzag vs. armchair) and its influence on local carrier concentration.[41] KPFM can be used to measure the local potential at edges, which enables interpretations of changes in local carrier concentration based on the Raman shifts.[83] Moreover, *in situ* transport measurements of FETs with encapsulated contacts (fabrication methods in Chapter 2 Section 2.6.2) can be conducted to assess the effects of functionalization on single-sheet properties during solution- or gas-phase processes. To investigate the influence of functionalization on junction characteristics, including near-edge and intersheet resistivities, a two-nanosheet model system can be designed, featuring a top nanosheet that overlaps with two buried edges of the bottom nanosheet, with one edge selectively patterned and functionalized (Figure 7.1). By comparing the field-effect characteristics and KPFM surface potential profiles of S-D1 and S-D2, it will be possible to determine which junction (with or without functionalization) limits device behavior; a lower potential drop is anticipated at the functionalized junction compared to the pristine one.
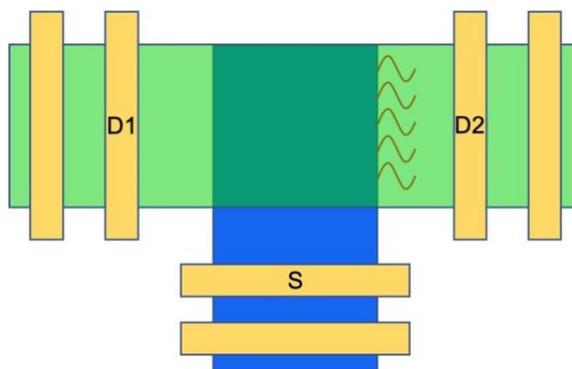
Figure 7.1. Schematic of a two-nanosheet model system with a functionalized buried edge.

7.2.2. Printed Optically Tunable Capacitor

As discussed in Chapter 4, optically tunable capacitors have applications in adjusting the resonance frequency in L/C circuits and fine-tuning reactance for impedance matching. The two primary figures of merit for these variable capacitors include the tuning ratio $\eta = C_{max}/C_{min}$, which represents the extent of modulation, and the quality factor $Q = \omega R_p C_p$ (for a parallel R/C circuit), which characterizes energy loss.[88] For optically tunable capacitors, rapid photoresponse (milliseconds) and capacitance memory effects (long retention time and cycle tolerance) are also desirable.

Polymer nanocomposites comprising a polymer matrix and semiconducting nanosheets may enable the development of printed optically tunable capacitors. In a nanocomposite consisting of high permittivity inorganic nanoparticles within a polymer matrix, where the nanoparticle diameter is significantly smaller compared to the composite thickness, interfacial polarization dominates due to charge accumulation at the polymer/inorganic interfaces when an electric field is applied (*i.e.*, the Maxwell-Wagner effect).[153,154] If the inorganic fillers generate a significant number of carriers upon illumination (*e.g.*, quantum dots and 2D nanoplates), the interfacial charge density

could increase, leading to enhanced interfacial polarization and thus a higher macroscopic permittivity. The challenge in processing is to prevent aggregation of 2D fillers, which may lead to local field concentration and subsequent dielectric breakdown.[155] Therefore, optimum nanosheet size, thickness, and density exist to simultaneously enhance photocapacitance and breakdown field. Photoimpedance spectroscopy with spatially resolved excitation can be employed to characterize the photoresponse of these devices.

7.2.3. Photoswitchable Memory in Printed vdW TFTs

Following the discussion in Chapter 6, the ion-binding property of specific photoswitches could be leveraged to enable optically modulated memory in printed TFTs with mixed ionic-electronic transport. A novel device concept could involve printed MoS_2 TFTs gated with a photoswitchable (polymeric) ionic liquid. In such a polymer composite, the ionic photoswitch derivatives would be attached to the polymer backbone and spatially separated. Photoisomerization could alter the electrostatic interaction between the counterion and the photoswitch, thereby changing the counterion mobility and the RC time constant of the composite. Segalman and colleagues synthesized a DAE-based photoswitchable ionic liquid, demonstrating anionic conductivity modulation upon UV/visible exposure.[143,144] Although the modulation of bulk conductivity currently takes tens of minutes, it is conceivable that the accumulation of ions at the semiconductor surface, driven by an applied gate electric field, could accelerate photoswitching at the interface and modulate the EDL capacitance.

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Appendix A   Laser Annealing of ALD-SnS$_2$

A.1. Introduction

Flexible electronics are typically fabricated by depositing and patterning circuits on flexible plastic substrates at low temperatures (<200 °C). Therefore, low-temperature deposition and processing techniques must be developed concurrently for 2D materials to enable their application in flexible electronics. Low-temperature atomic layer deposition (ALD) allows for direct, patternable growth of continuous transition metal dichalcogenide (TMD) films onto plastic substrates. However, TMDs synthesized at low temperatures may be amorphous or nanocrystalline, limiting their electronic mobility. While thermal annealing can crystallize amorphous TMDs, the annealing temperatures (>200 °C) are incompatible with typical flexible substrates. In contrast, brief laser irradiation offers a viable method for achieving locally confined modifications of TMDs without damaging the substrate. In our study, we used ALD-grown SnS$_2$ as a prototype TMD material to elucidate the relationship between microstructure and electronic performance as it evolves with laser annealing conditions in controlled environments.

A.2. Methods

Laser annealing of ALD-SnS$_2$ was investigated using Raman spectroscopy and field-effect transistor (FET) measurements. Devices were fabricated by pre-patterning contacts on substrates. Amorphous SnS$_2$ thin films (nominally 10 nm) were grown on SiO$_2$/Si or Si$_3$N$_4$/Si substrates by ALD at 120 °C and encapsulated with AlO$_x$ (nominally 5 nm) in situ. A continuous-wave laser with a wavelength of 532 nm and a spot size of approximately 1 μm was scanned over ALD-SnS$_2$

with a 250 nm step size at various powers and durations. Subsequently, Raman maps of the laser-annealed regions were obtained at 300 µW with an integration time of 0.5 s (Figure A.1).
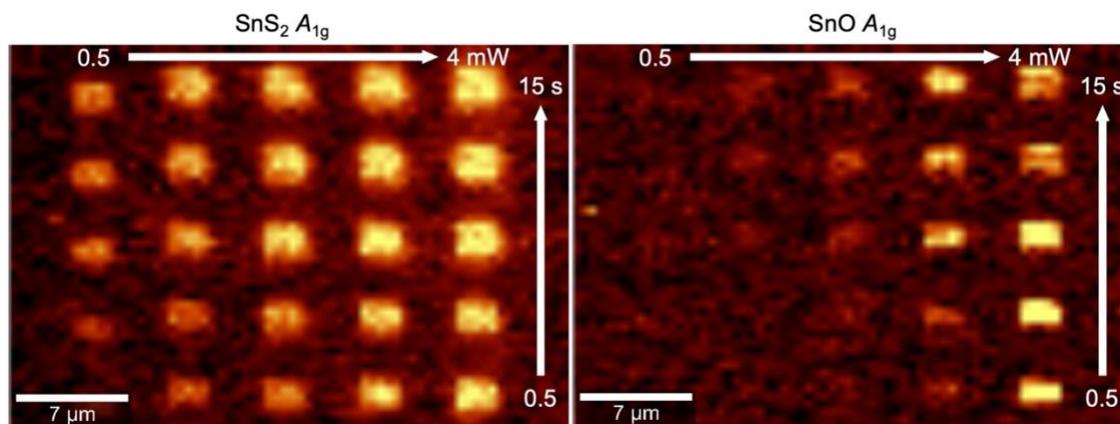
Figure A.1. Raman maps of SnS₂ (left) and SnO (right) A_{1g} intensities of ALD-SnS₂ annealed with different laser powers and durations.

A.3. Results and Discussion

Laser annealing increases the intensity of SnS₂ A_{1g} mode, with higher annealing power resulting in higher SnS₂ Raman intensity (Figure A.2a,b). This suggests that higher laser annealing power may promote faster diffusion of SnS₂ crystallites to form larger grains. However, laser annealing SnS₂ on SiO_2/Si induces formation of SnO with increasing annealing power (Figure A.2a), while annealing on Si_3N_4/Si seems to suppress the extent of oxidation (Figure A.2b), which suggests that an oxygen-free interface is essential for producing phase pure SnS₂ by annealing. Moreover, laser annealing transforms the as-grown insulating film into a n-type semiconductor, which exhibits higher field-effect (FE) mobility at higher annealing power (Figure A.2c,d). Additionally, the SnS₂ FETs on SiO_2/Si demonstrate significantly higher mobilities than those on

Si$_3$N$_4$/Si, which indicates that the oxidation of SnS$_2$ may contribute to the improved FE mobility. Thus, the FE effect mobility of laser-annealed ALD SnS$_2$ is correlated with both the annealing conditions and the substrate properties. These preliminary results show that laser annealing is a viable approach to spatially recrystallize amorphous SnS$_2$ into a n-type semiconductor with enhanced FE mobility.
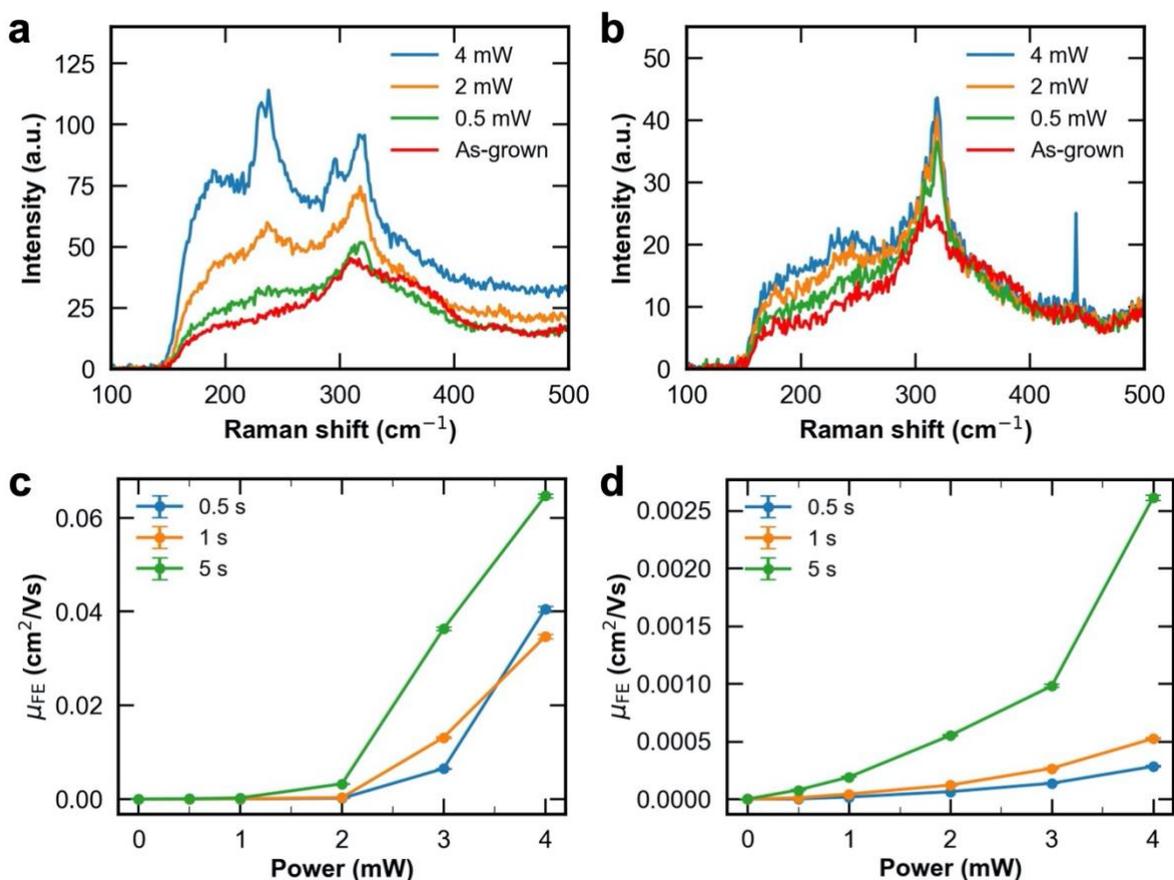
Figure A.2. Raman and FET characterizations of laser-annealed SnS$_2$. Raman spectra versus annealing powers of films grown on (a) SiO$_2$/Si and (b) Si$_3$N$_4$/Si. All spectra were normalized by the integrated intensity of the Si peak. Field-effect mobilities μ_{FE} versus annealing powers and times of films grown on (c) SiO$_2$/Si and (d) Si$_3$N$_4$/Si.